

# MS-7B89 Ver:2 1

## CPU:

AMD AM4

## System Chipset:

Promontory B450

(Value DIY or System Builder)

## Main Memory:

DDR IV \* 4 MAX 64GB

## VRM

RI8894 4+2

## On Board Chipset:

LPC Super IO -- NCT6795D

LAN RTL8111H

Azalia CODEC - Realtek ALC892

## Expansion Slots:

From CPU

PCI Express X16 Slot \* 1

From FCH

PCI Express X1 Slot \* 1

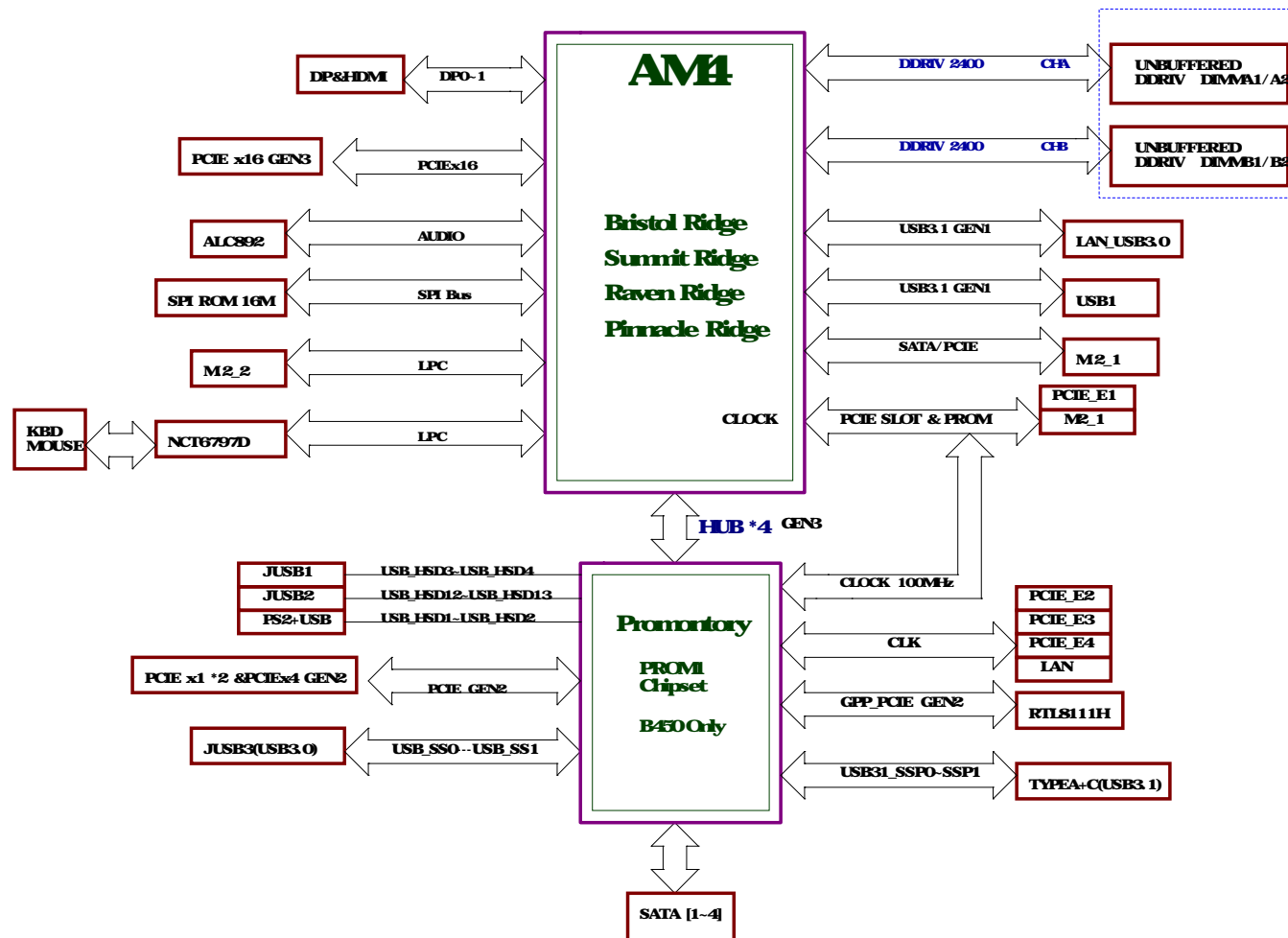
PCI Express X1 Slot \* 1

PCI Express X1 Slot \* 4

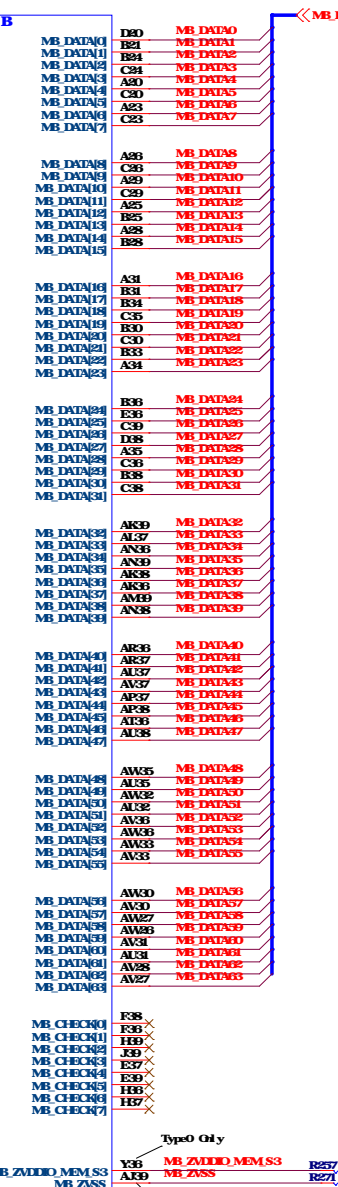
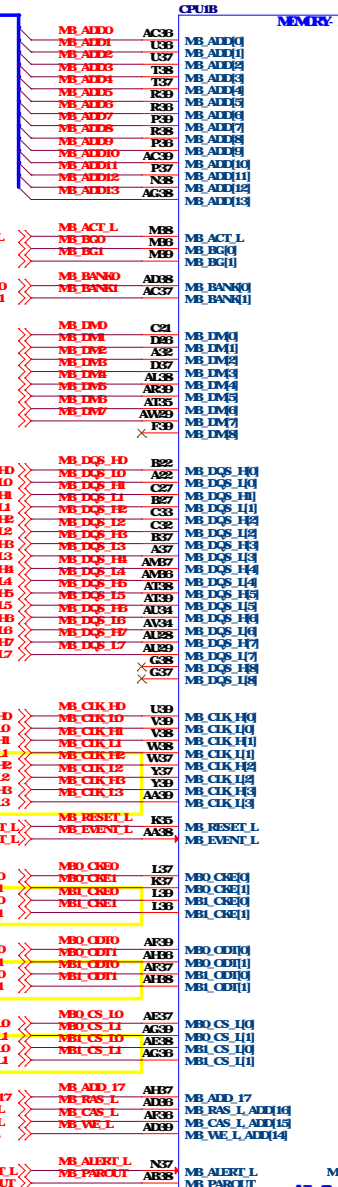
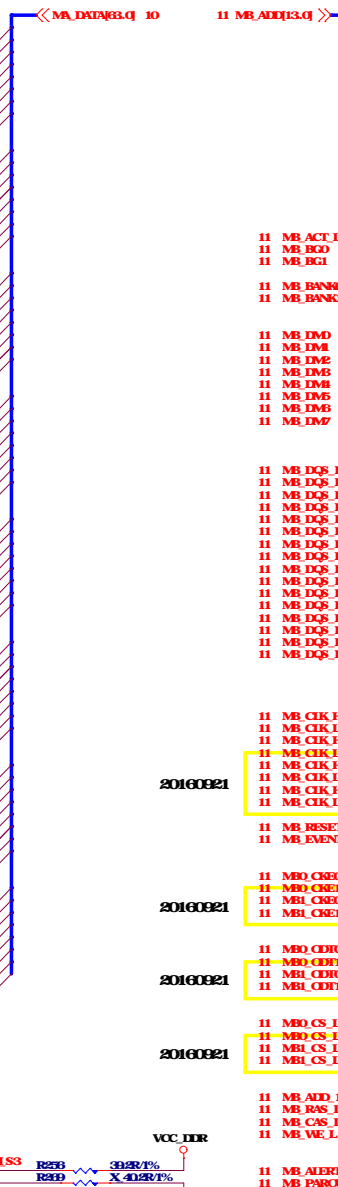
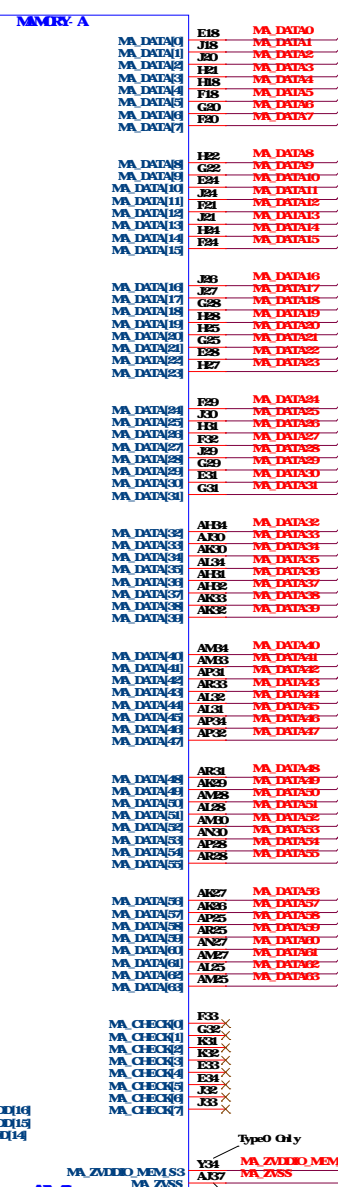
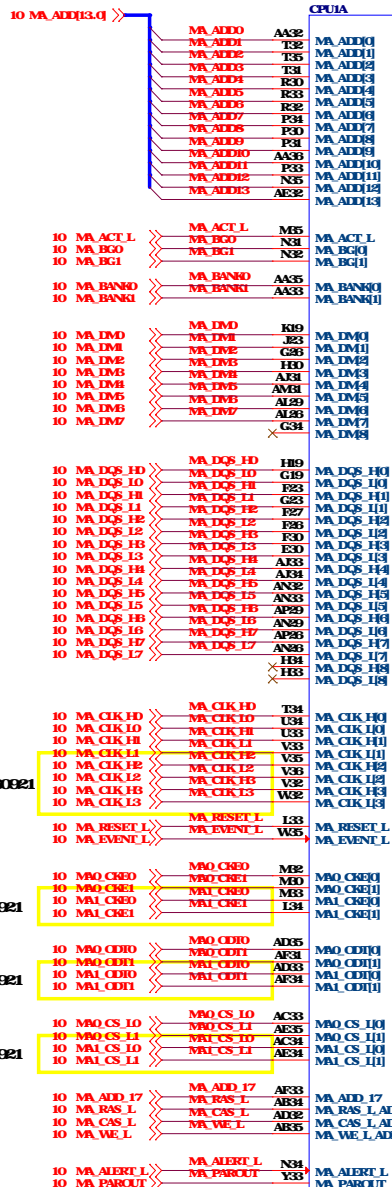
## OCPU IC:

RI9553B

## FUSION BLOCK DIAGRAM

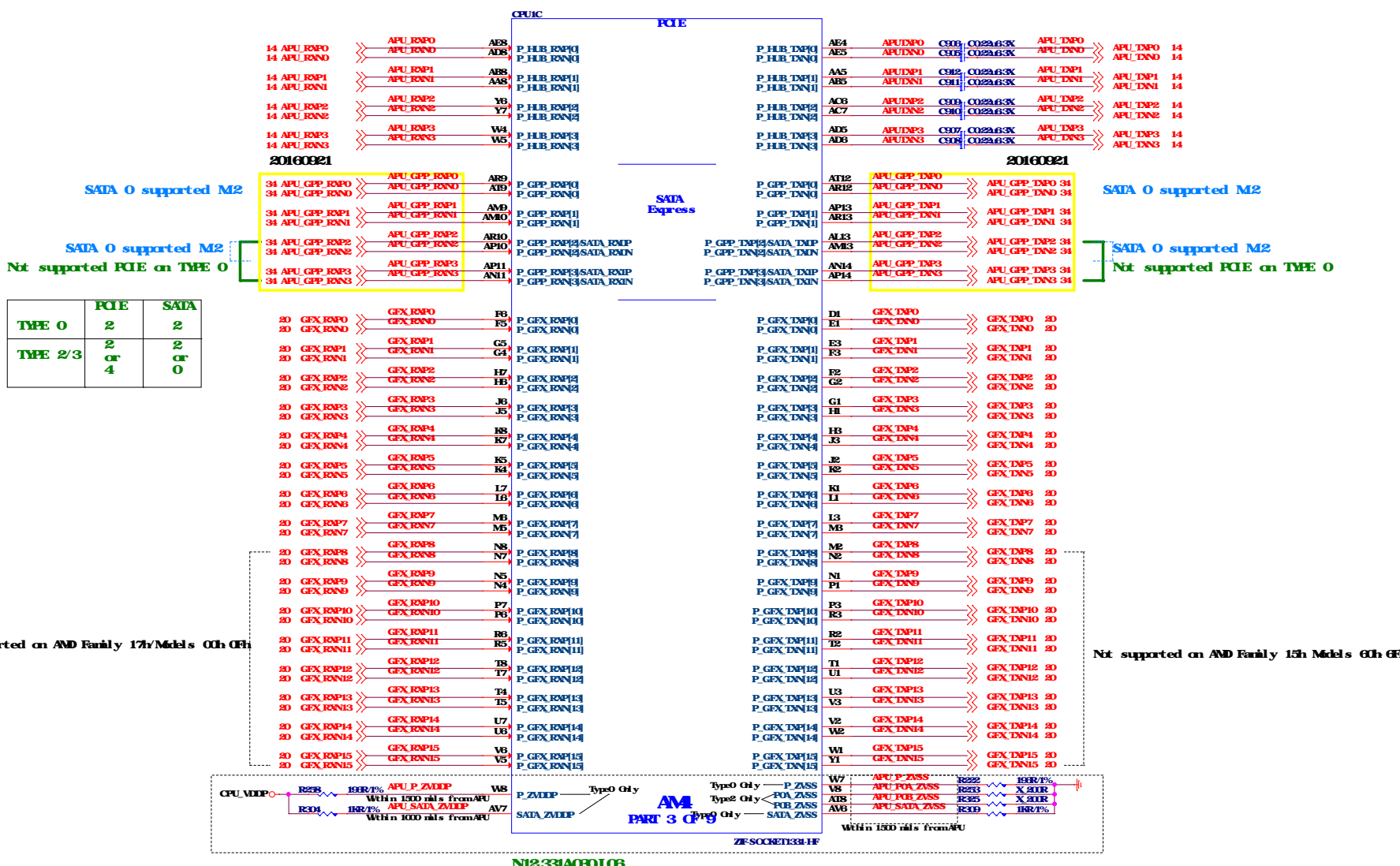


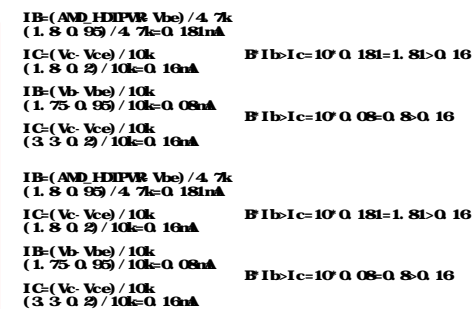
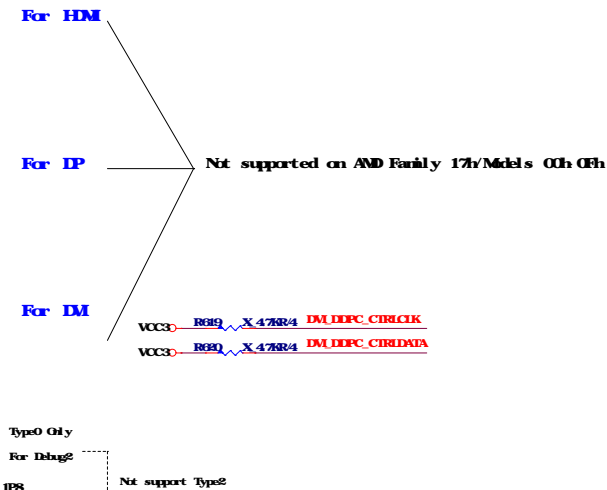
<b>01 Block Diagram</b>	<b>31 Rear USB3.1 TYPE C</b>
<b>02 Cover Sheet</b>	<b>32 USB Front Side</b>
<b>03 AM4 DDR4 IF</b>	<b>33 USB Front JUSB4</b>
<b>04 AM4 PCIe/SATAE</b>	<b>34 M2</b>
<b>05 AM4 Display/Audio</b>	<b>35 SATA Connector</b>
<b>06 AM4 SMI/ACPI/GPIO</b>	<b>36 DP</b>
<b>07 AM4 IPC/SPI/USB/CLK/STRAP</b>	<b>37 DMI Connector</b>
<b>08 AM4 Power/RTC Power</b>	<b>38 HDMI</b>
<b>09 AM4 GND</b>	<b>39 ACPI uPI 5V DIMM R3/USB</b>
<b>10 DDR4 DIMMCHA</b>	<b>40 PMNB671GD 1.05V/GS7133 2.5V</b>
<b>11 DDR4 DIMMCHB</b>	<b>41 DDR PWR VPP25V/TT_DDR</b>
<b>12 DDR4 POWER/GND 1</b>	<b>42 DDR4 S125E Power</b>
<b>13 DDR4 POWER/GND 2</b>	<b>43 CPU Power IP8V/MP2147</b>
<b>14 Promontory PCIe/SATA/SATAE</b>	<b>44 CPU Power VDDP-RTS125E</b>
<b>15 Promontory USB/OC</b>	<b>45 CPU Power Connector/PWRGD</b>
<b>16 Promontory CLK/ACPI/GPIO</b>	<b>46 CPU Power RT8804 4+2 Phase</b>
<b>17 Promontory Power</b>	<b>47 CPU Power Phase 1-3</b>
<b>18 Promontory GND</b>	<b>48 CPU Power Phase 4</b>
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N1233A0B0106

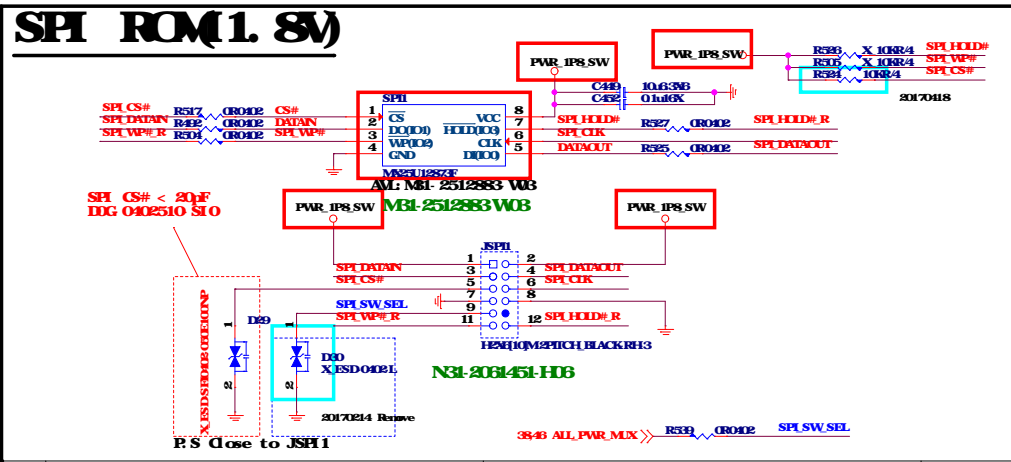
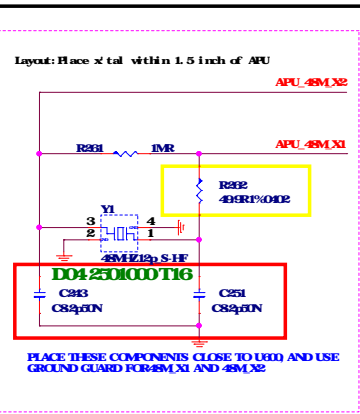
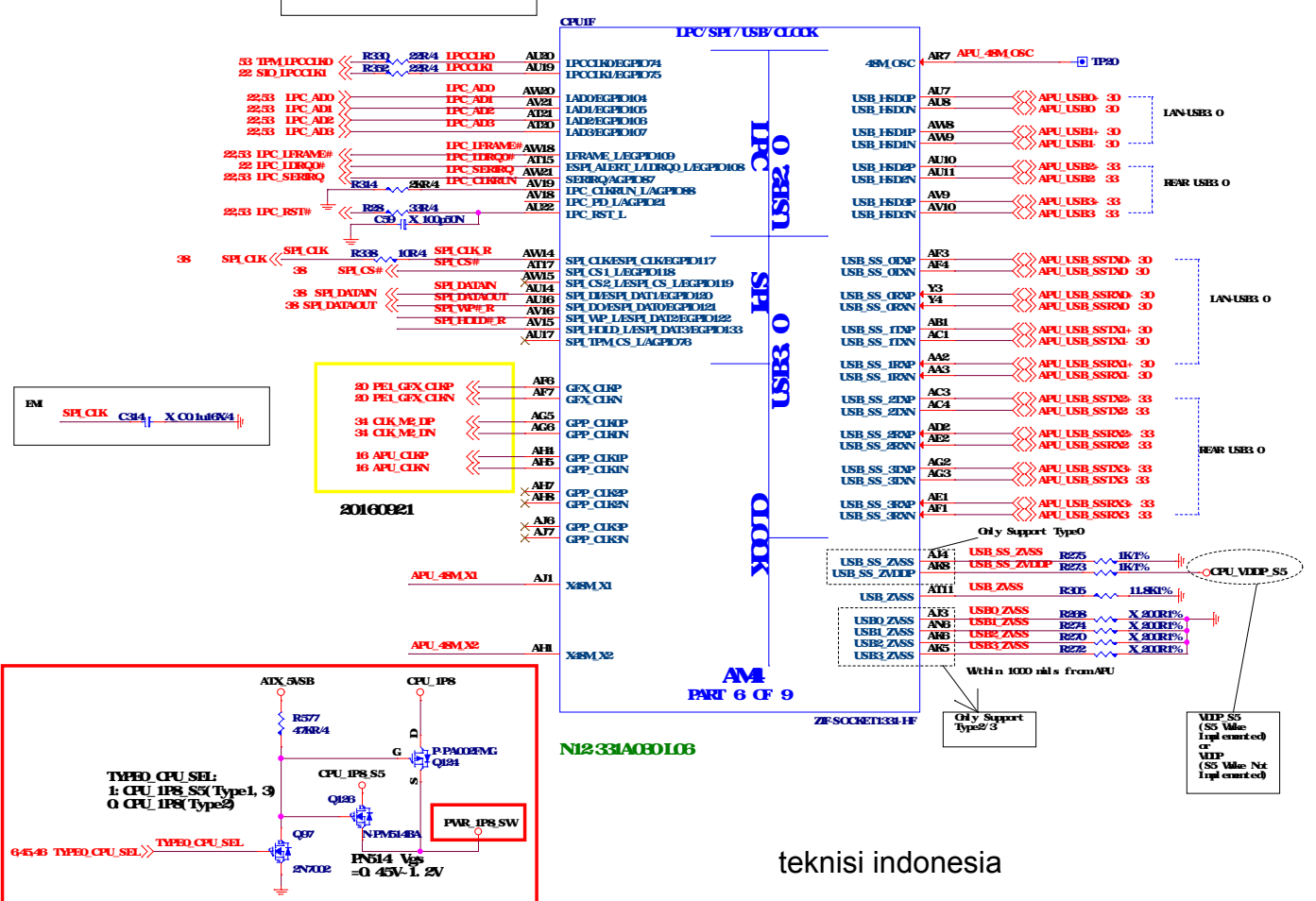
N1233A0B0106



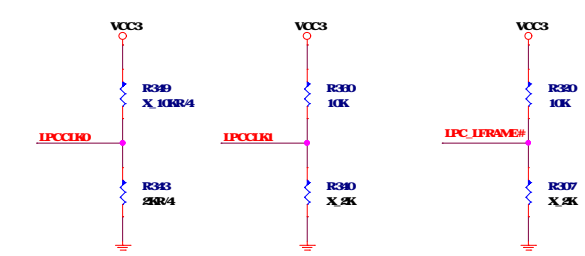




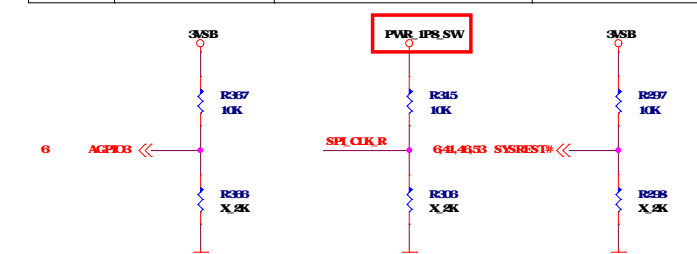




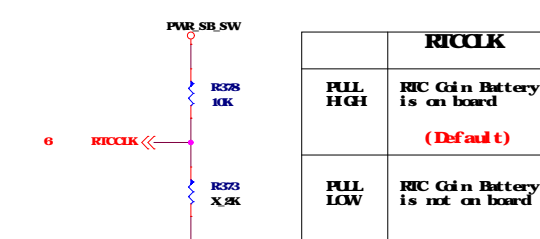
## Strapping Options



	IPCOLK0	IPCOLK1	SIO_LFRAME
PULL HIGH	IPC device Boot Fail Timer Enabled	Configured for Internal clock generator  (Default t)	SH ROM  (Default t)
PULL LOW	IPC device Boot Fail Timer Disabled  (Default t)	Configured for External clock generator ?????	IPC ROM



	AGPIOB	SPI_CLK	SYSEST#
PULL HIGH	Enhanced Reset Logic  (Default)	Use 48MHz crystal clock and generate both internal and external clocks  (Default)	Normal reset mode  (Default)
PULL LOW	Traditional Reset Logic	Use 100MHz PCIe clock as reference clock and generate internal clocks only	short reset mode



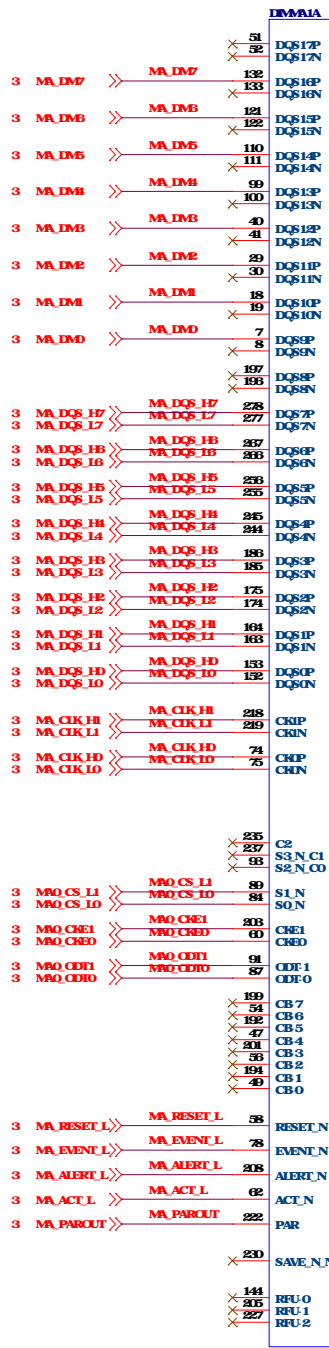
	<b>RICK</b>
<b>PULL HIGH</b>	<b>RIC Gain Battery is on board</b>  <b>(Default)</b>
<b>PULL LOW</b>	<b>RIC Gain Battery is not on board</b>





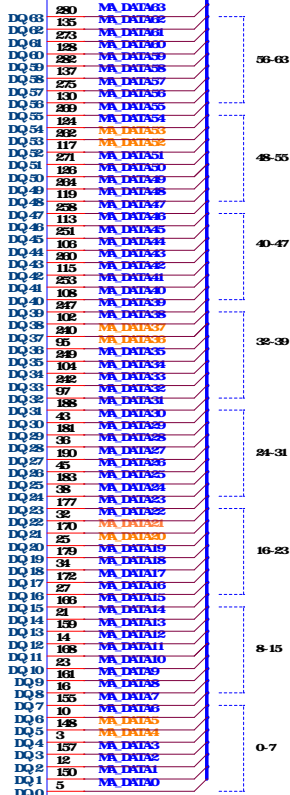


A1 A2 B1 B2



DIMM0:28P BLACKH121

N13280F81-L03

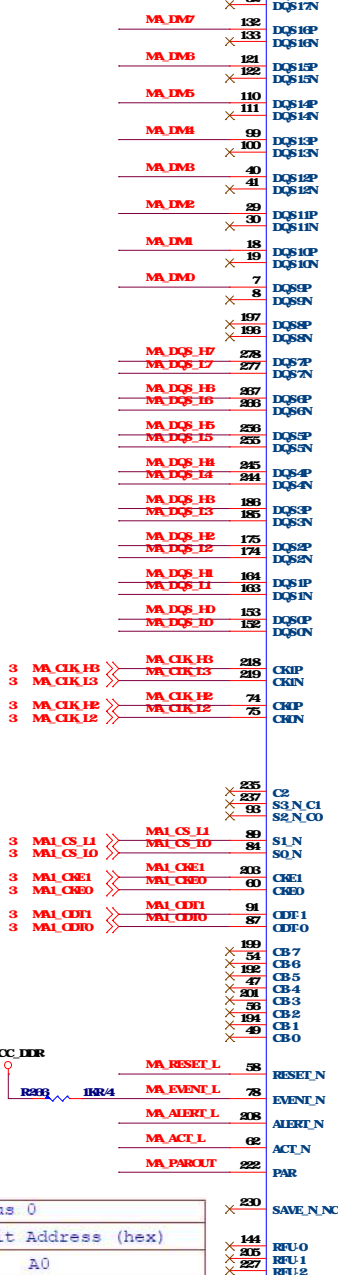


DIMM( CHANNEL A) - A0  
ADDRESS = 0 0 [SAI: SA0]

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMA1	A4
DIMMB0	A2
DIMMB1	A6

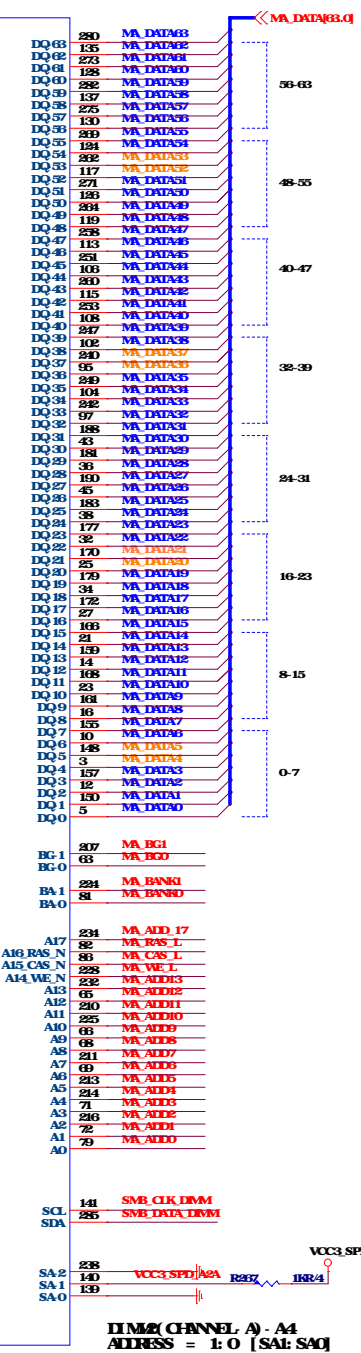
G3L3847L5L57 SC1D0 >> SC1D0 R27 >> R27 R4 >> R4 SMC\_CLK\_DIMM >> SMC\_CLK\_DIMM 11  
G3L3847L5L57 SD1D0 >> SD1D0 R43 >> R43 R4 >> R4 SMC\_DATA\_DIMM >> SMC\_DATA\_DIMM 11

DIMMA2



DIMM0:28P BLACKH121

N13280F81-L03



DIMM2( CHANNEL A) - A4  
ADDRESS = 1 0 [SAI: SA0]

MSI MICROSTART INFL CO., LTD.

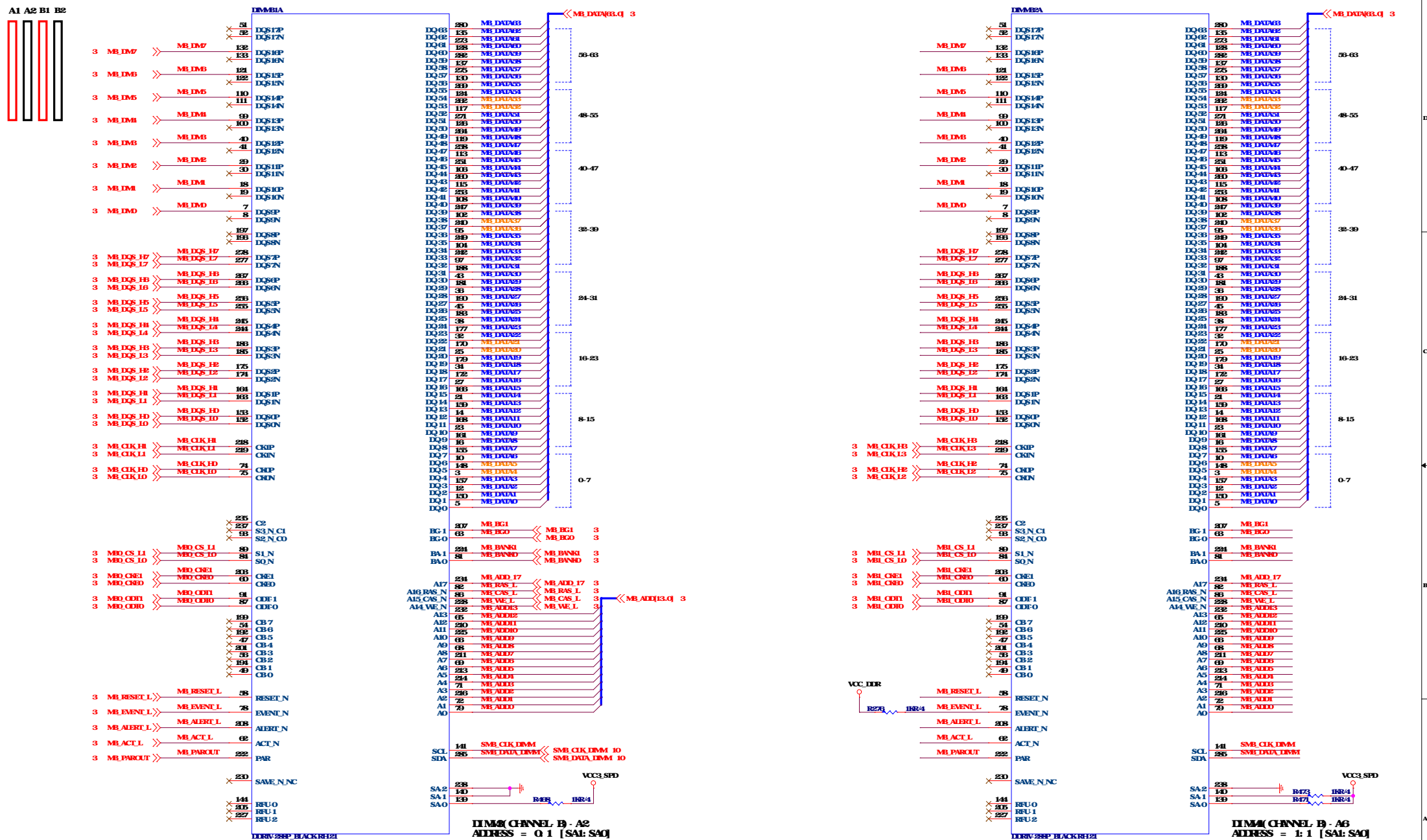
DIR4DIMMCHA

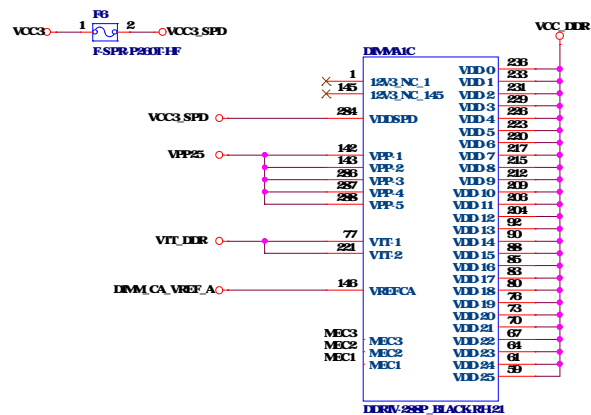
Document Number: MS-7889

Rev: 21

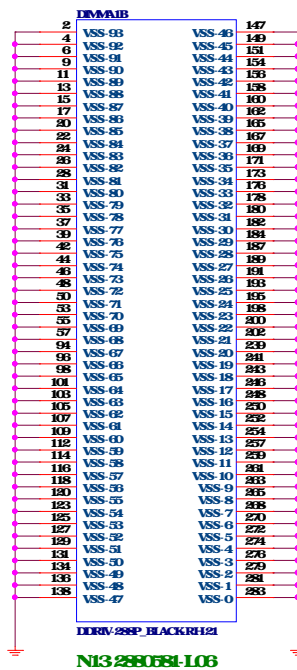
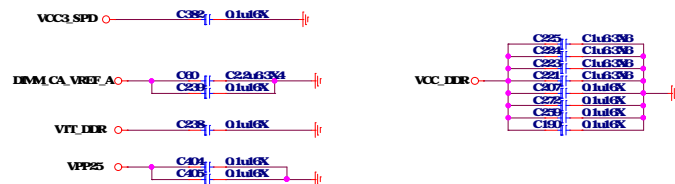
Date: Wednesday, July 04, 2006

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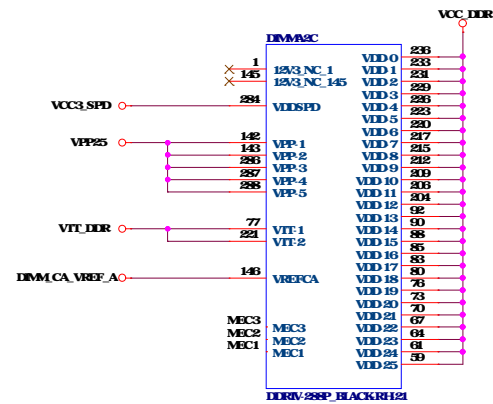


**N13 2880581-L06**

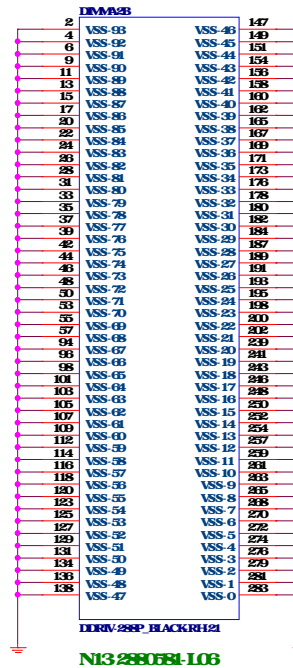
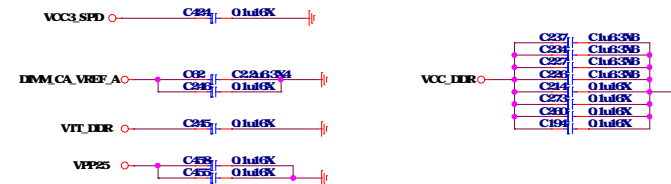


**N13 2880581-L06**

### DIMMSLOT PN BY SPEC



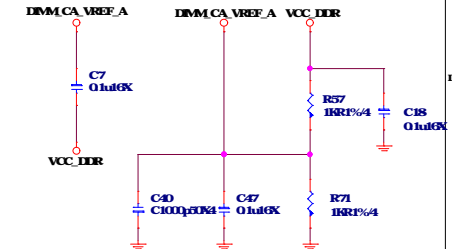
**N13 2880581-L06**

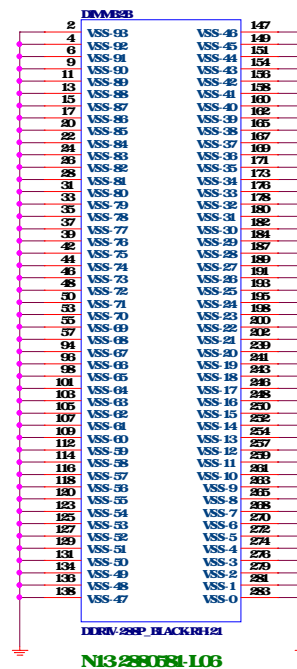
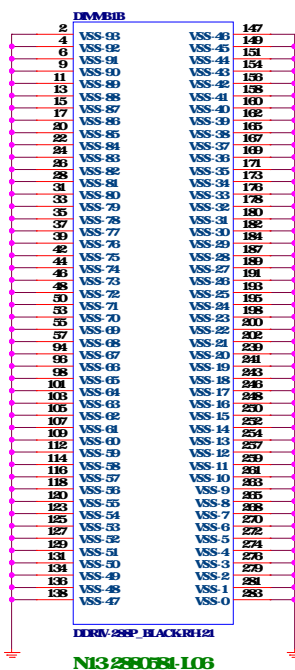
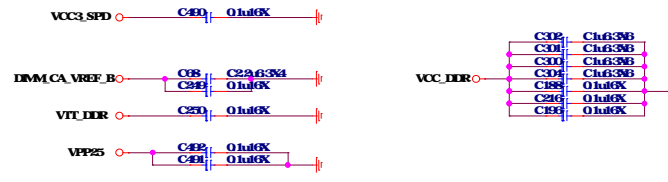
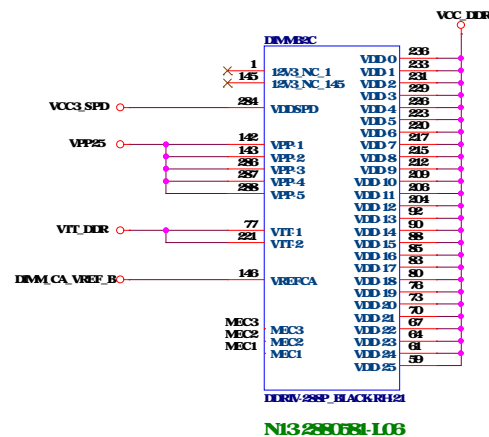
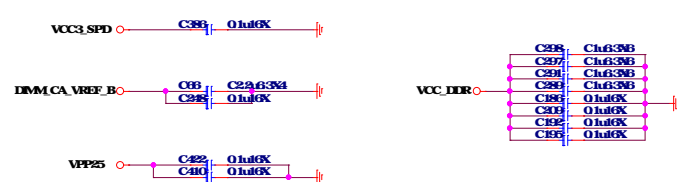
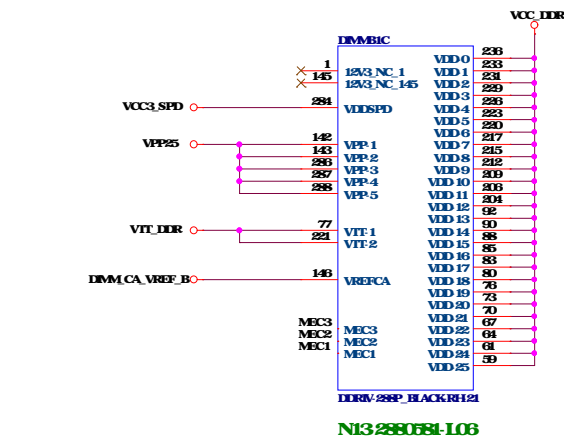


**N13 2880581-L06**

## DDR VREF

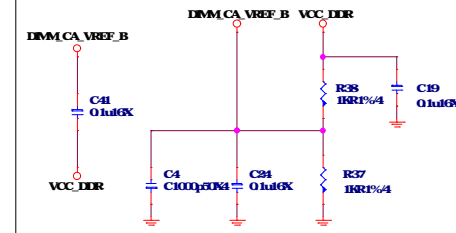
**(place resistors close to DIMMs)**





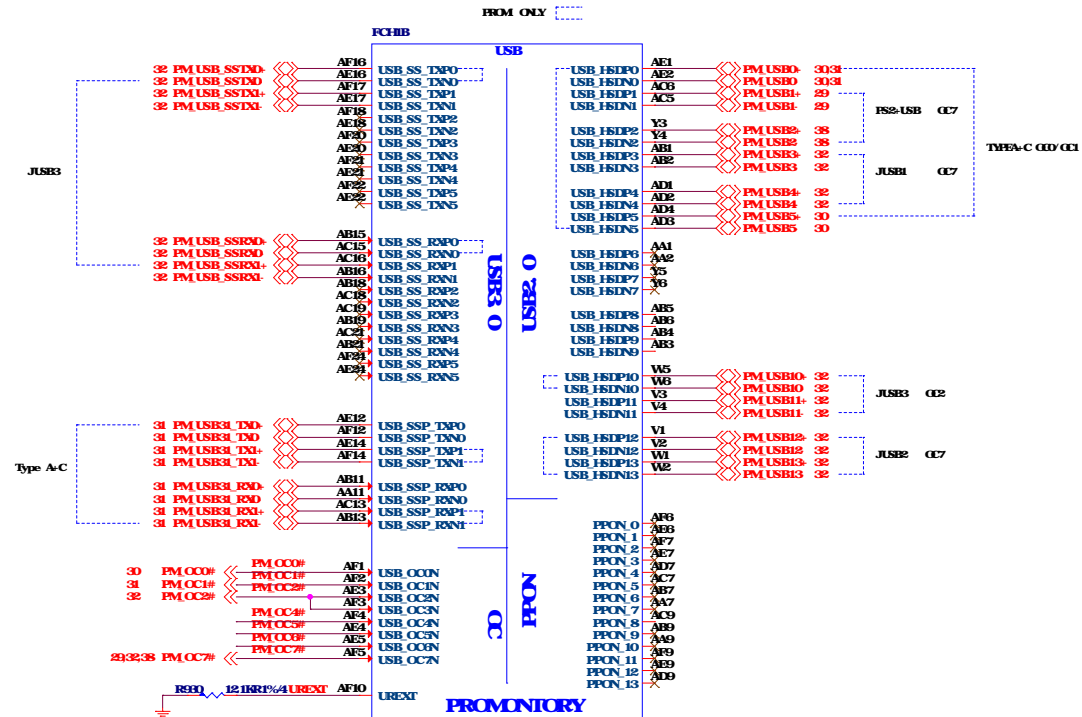
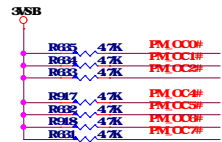
## DDR VREF

(place resistors close to DIMMs)



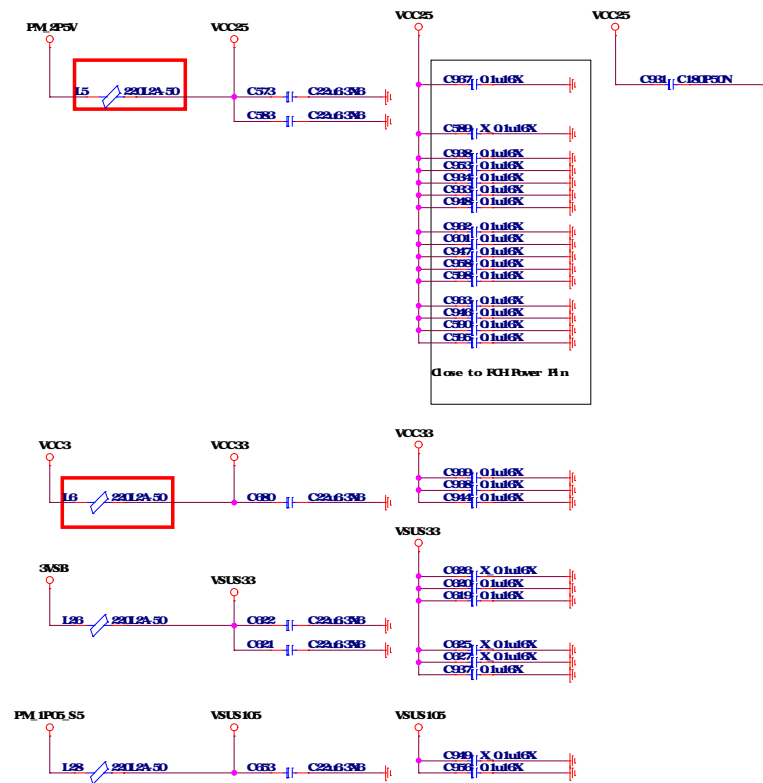
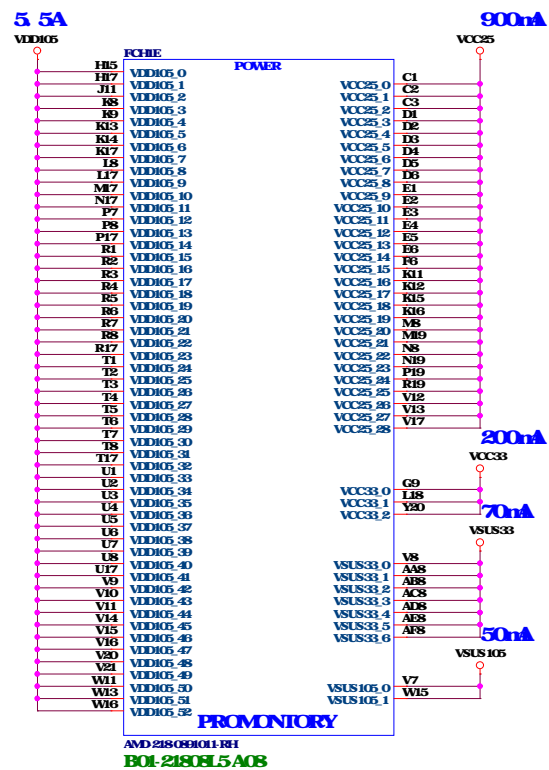
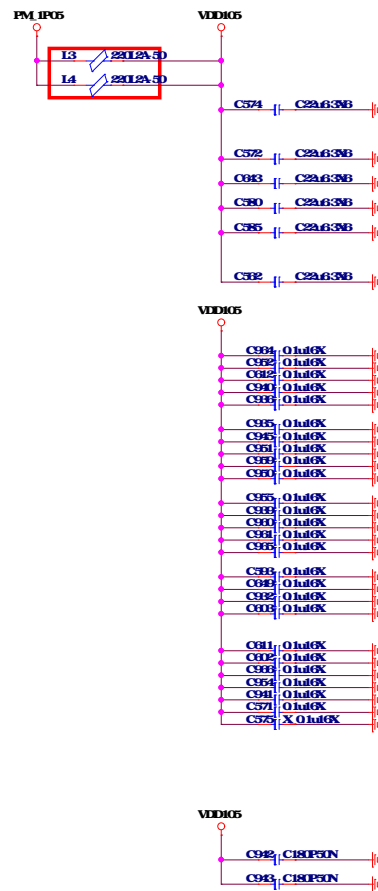


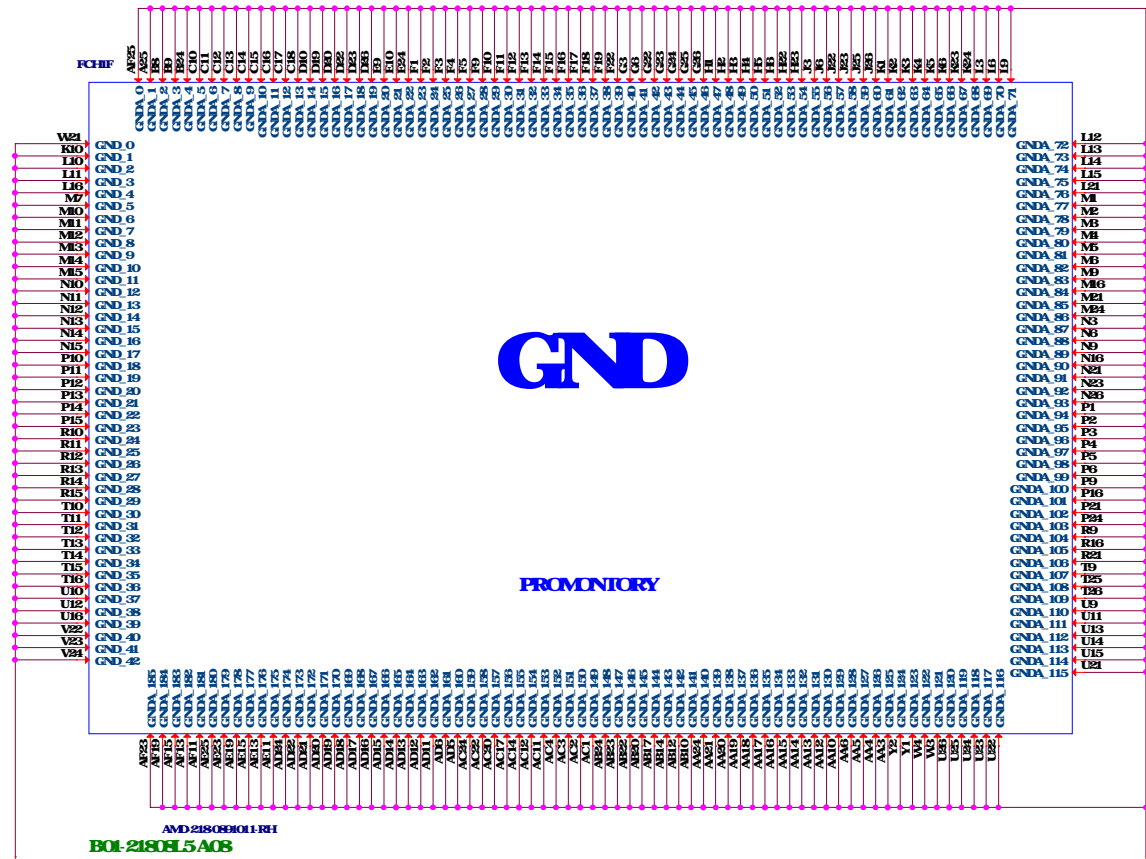




AMD21808011.FH1  
BOL-2180L5A08





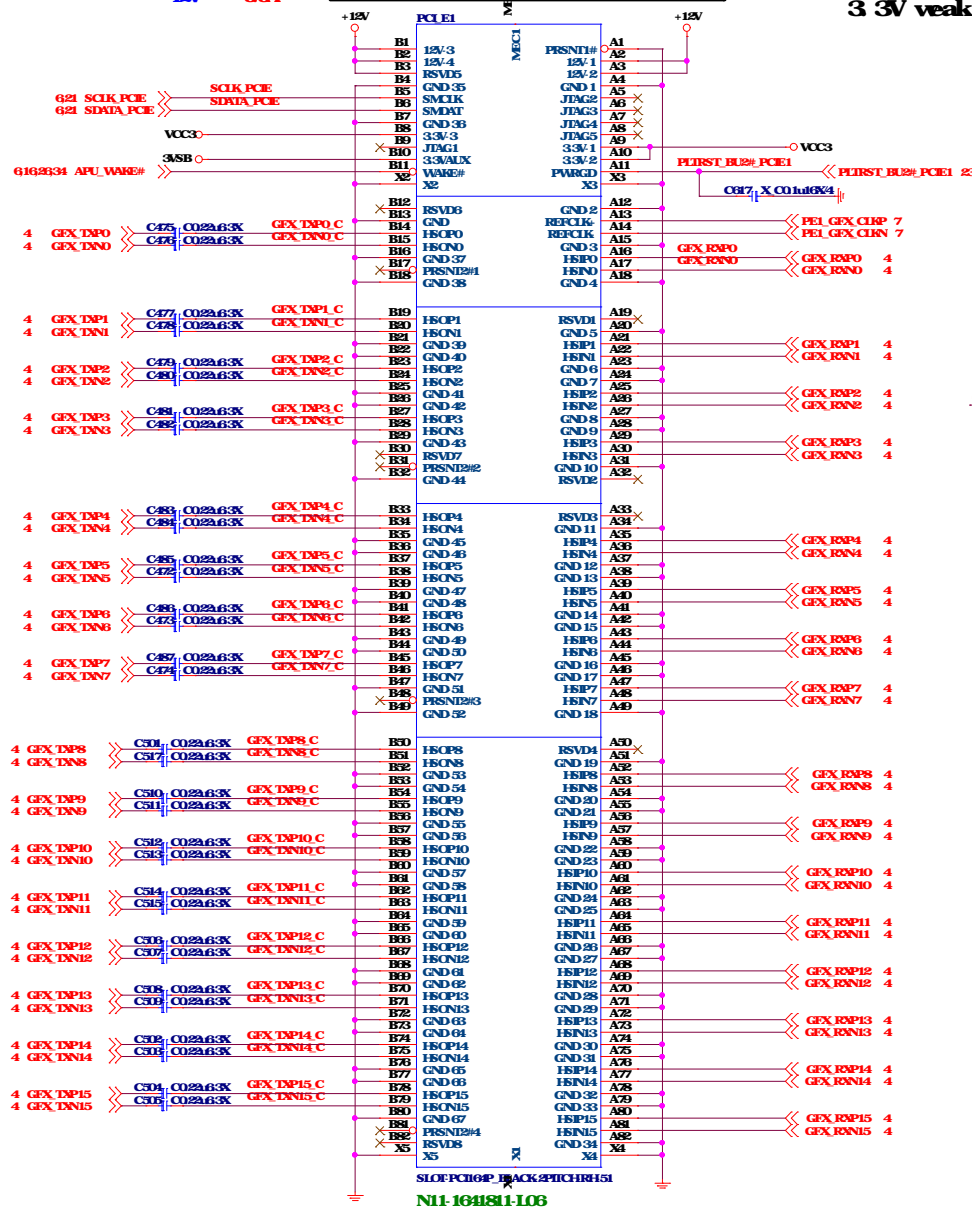




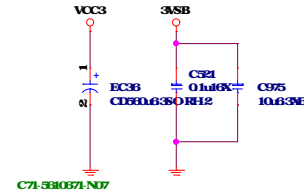
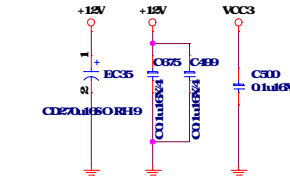
3.3V 30A  
12V 5.5A

# PCI EXPRESS x16 Slot

PCIEX1 12V 0.5A  
3.3V weak 375mA

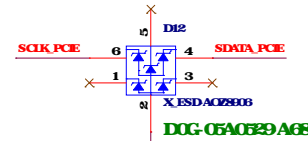


C7A-271170-N07



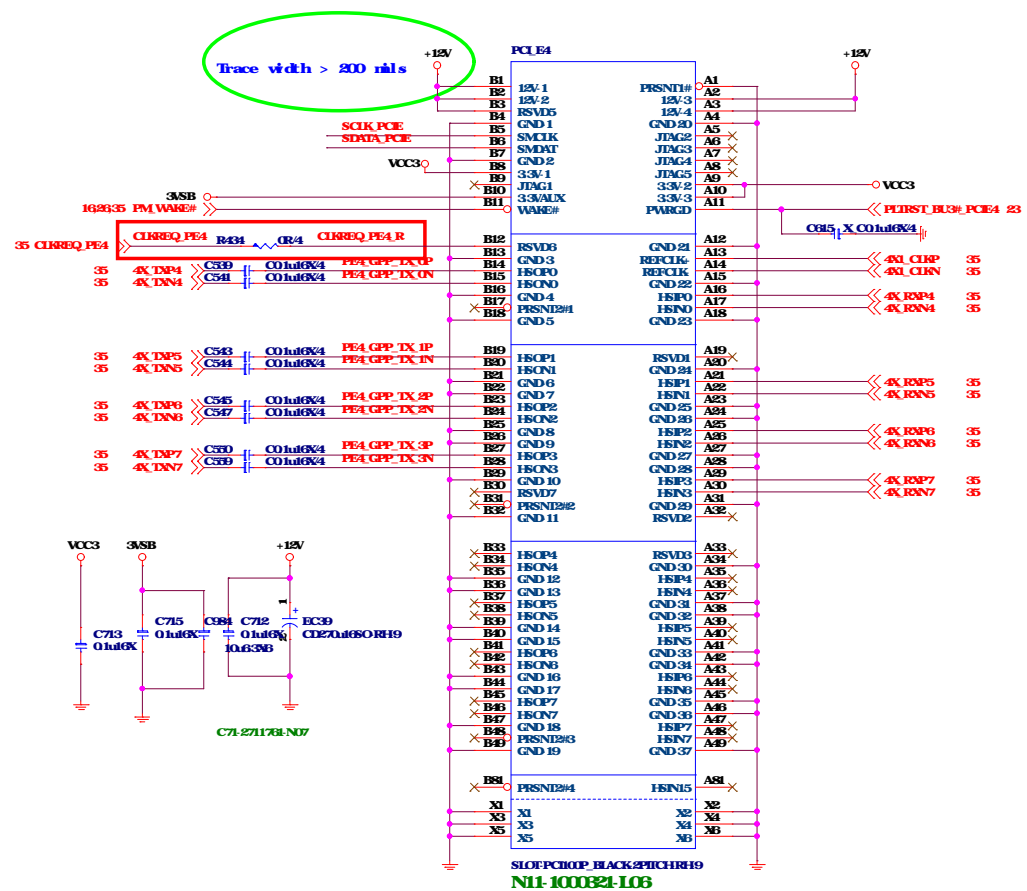
C7A-581071-N07

## SMBus separate circuit

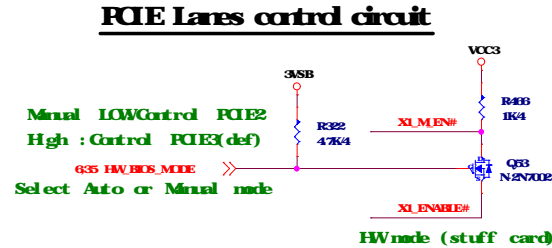


SMB SEL  
GHO Default High

**33V**      **30A**  
**12V**      **05A**



```
default (H: (PCI2)
Low (On+/- )=>(PCI3)
High(Ob+/- )=>(PCI2)
```

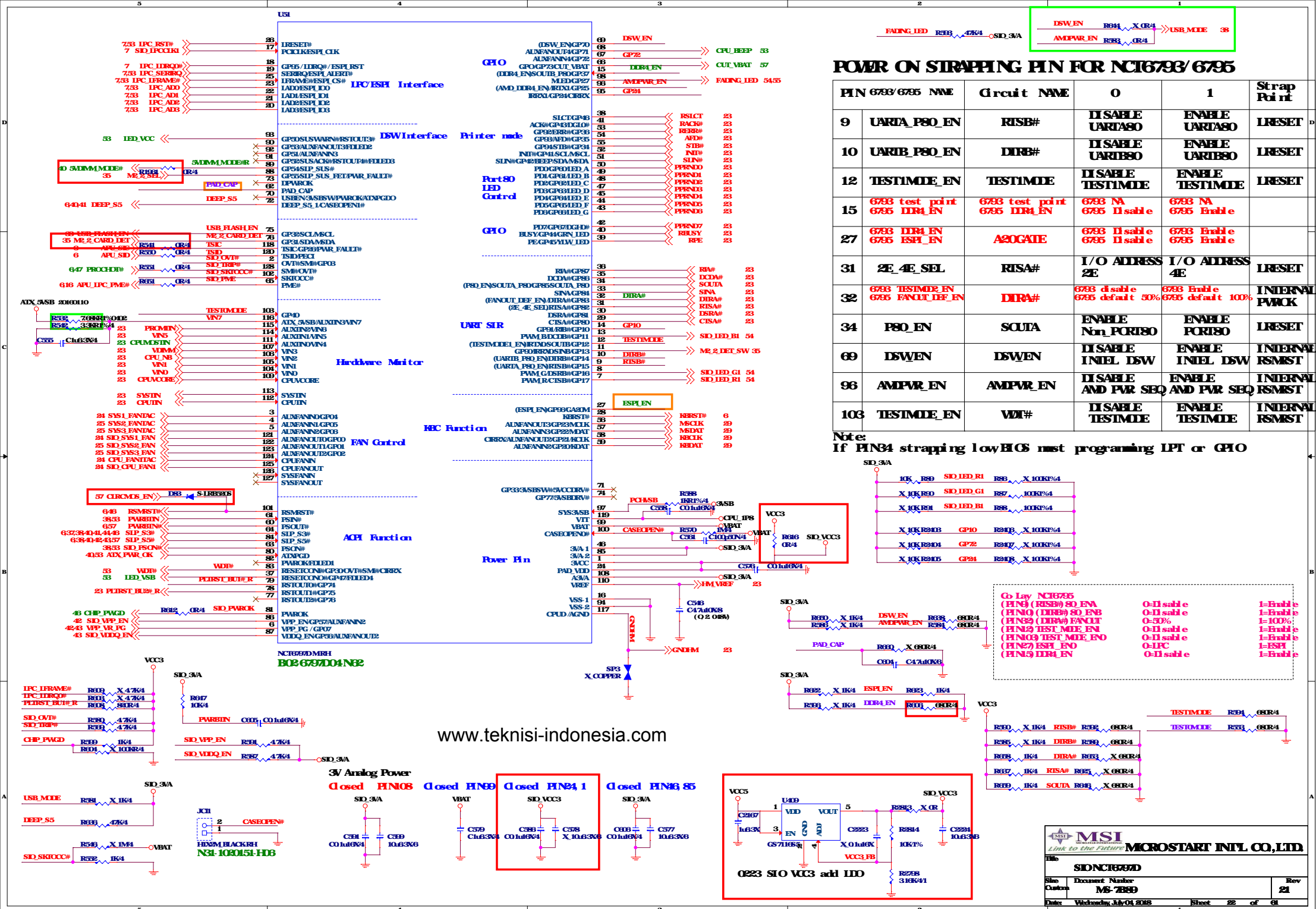


**PCI Express x4 Slot\*1**

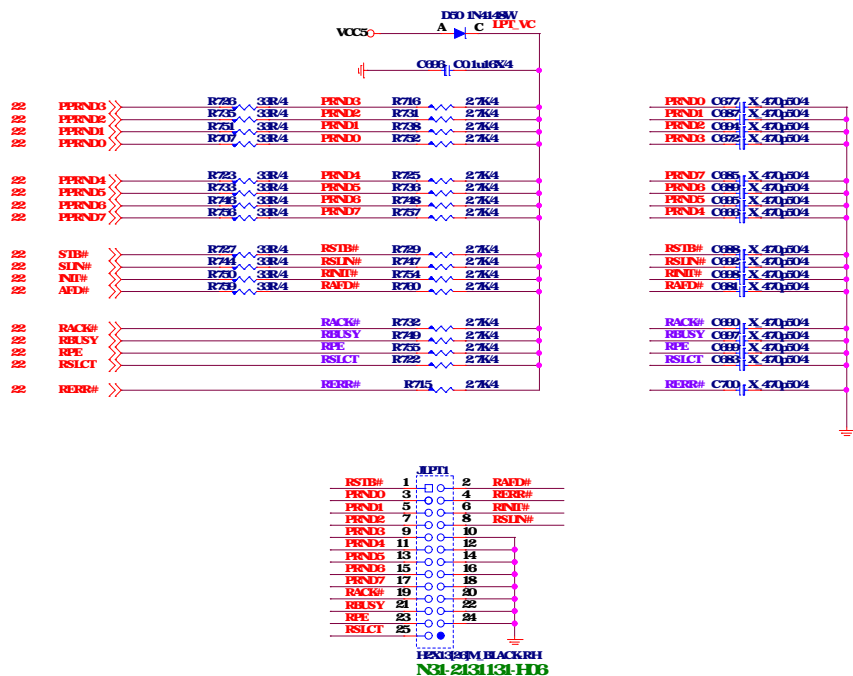
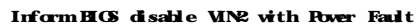
<b>+12V</b>		<b>- 21A</b>
<b>+VCC3</b>		<b>- 3A</b>
<b>+3V3_S5</b>	<b>(wake)</b>	<b>- 375mA</b>
<b>+3V3_S5</b>	<b>(nowake)</b>	<b>- 20mA</b>
<b>PCI Express x1 Slt*2</b>		
<b>+12V</b>		<b>- 1A</b>
<b>+VCC3</b>		<b>- 6A</b>
<b>+3V3_S5</b>	<b>(wake)</b>	<b>- 750mA</b>
<b>+3V3_S5</b>	<b>(nowake)</b>	<b>- 40mA</b>

**Title** **POE X4(XI\*2) SLOT**

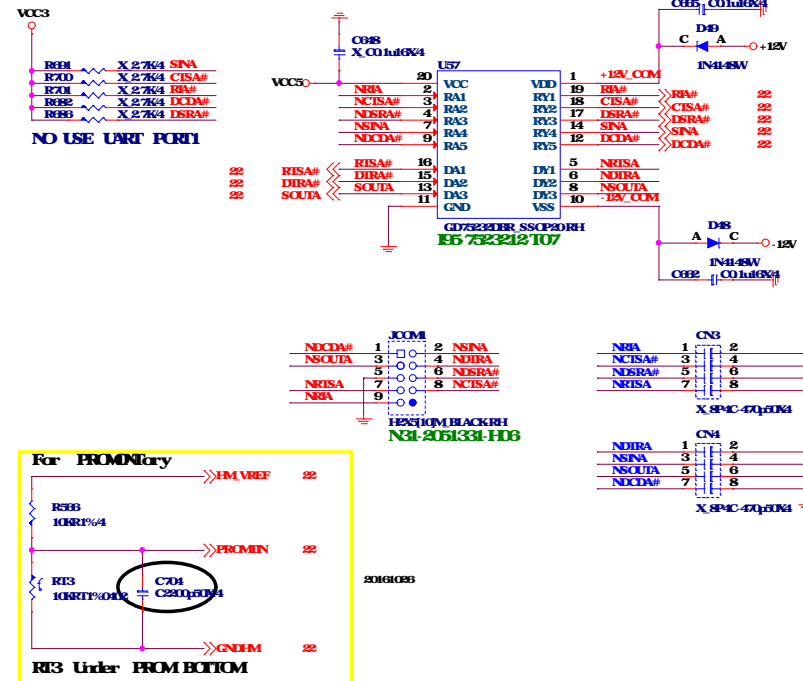
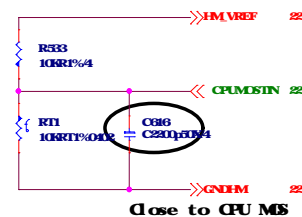
Site Custom	Document Number <b>MS-789</b>	Rev <b>21</b>
Date	Wednesday, July 04, 2018	Sheet 21 of 61



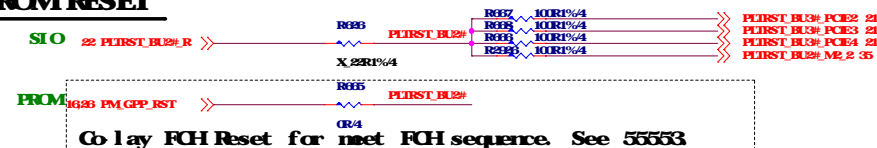
**SIO HM Voltage over 2.048V will not detect**



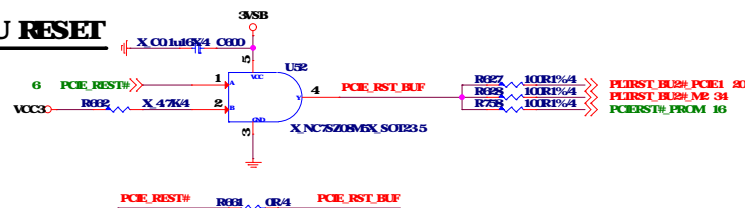
## COM PORT



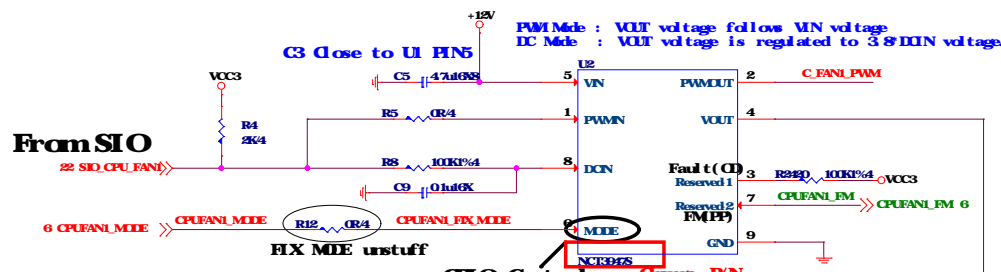
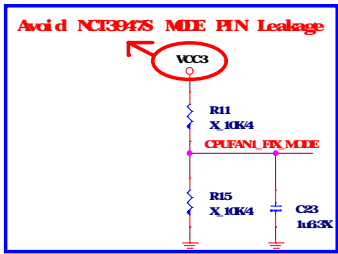
## FROM RESET



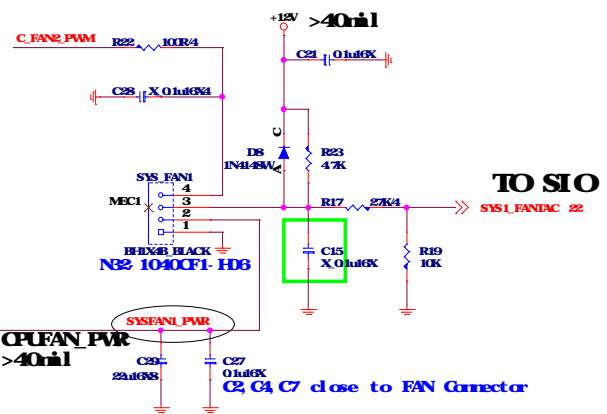
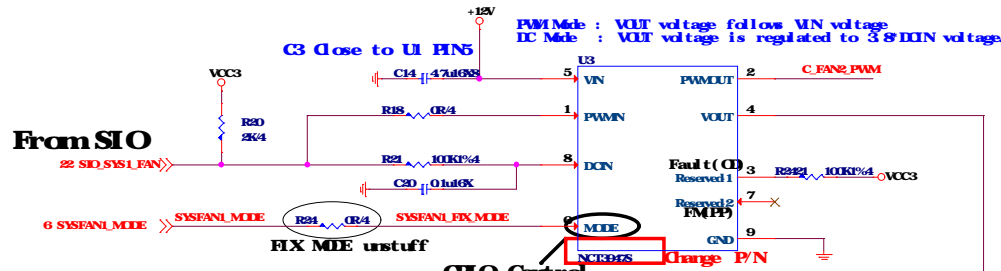
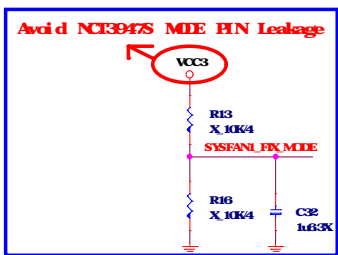
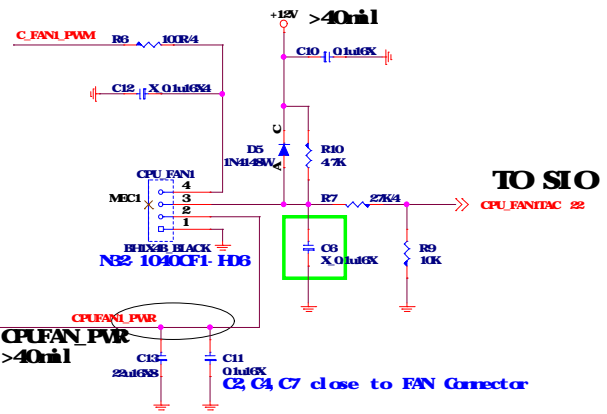
## CPU RESET



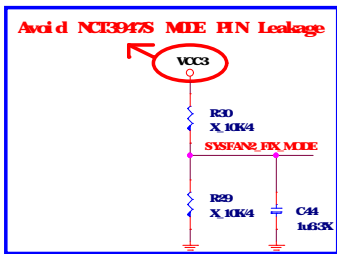
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MDE  
2 GPIO BD PW MDC MODE



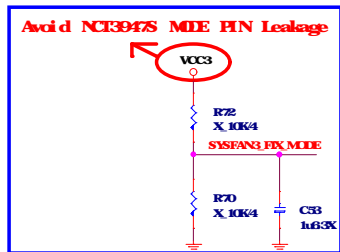
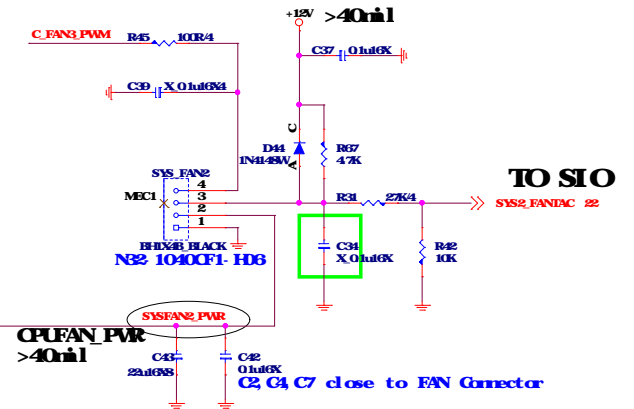
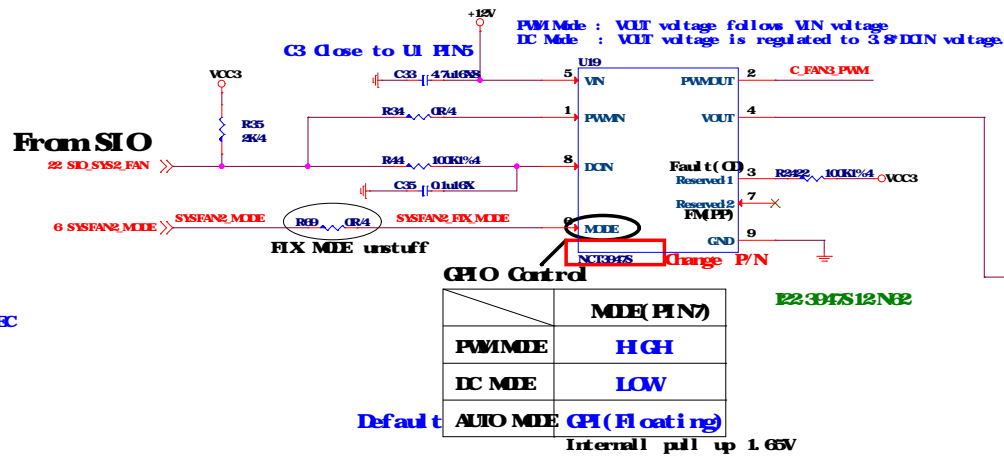
teknisi indonesia



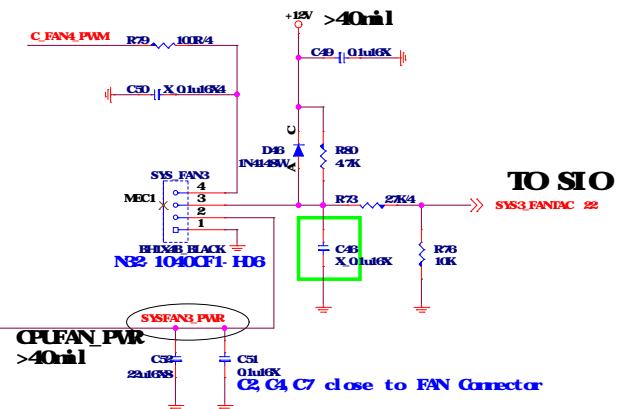
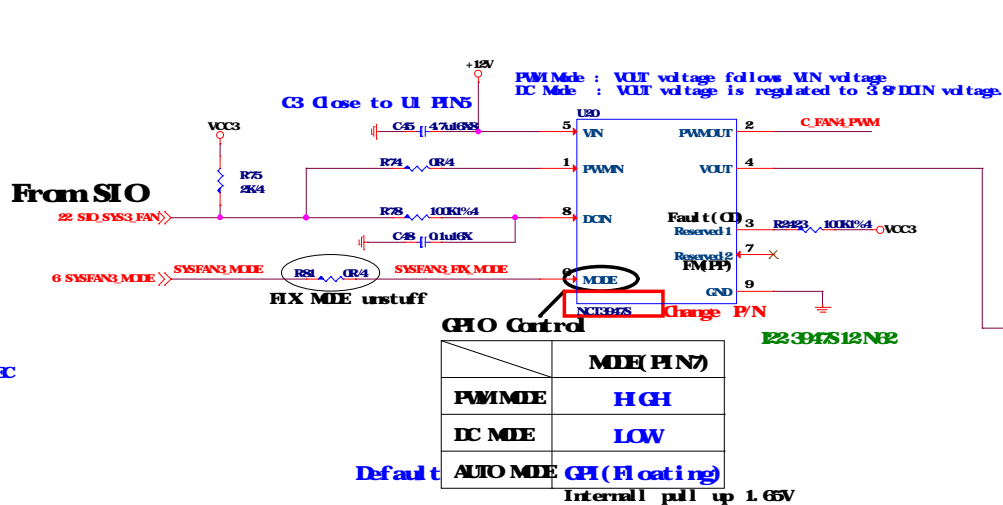




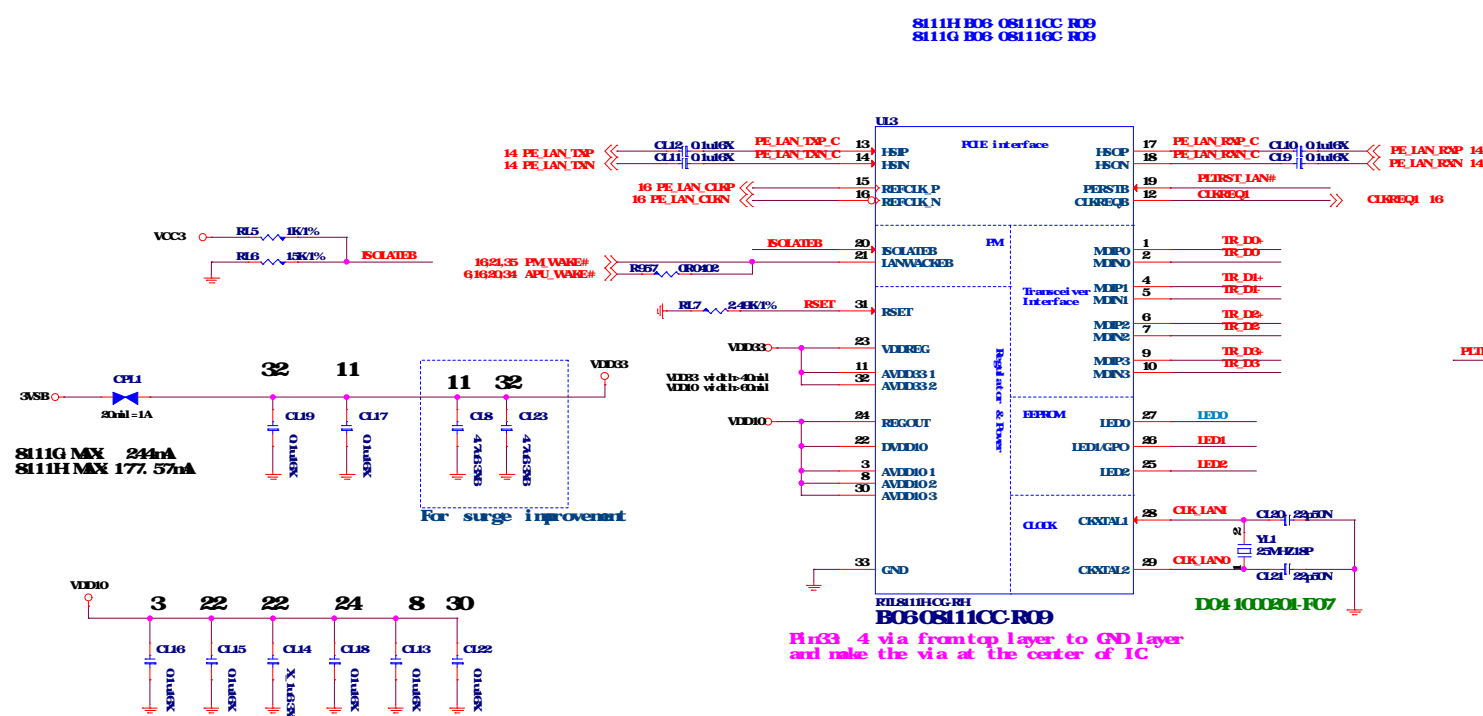
Reserve For FLX TC or PWM MDE USE By PMSPEC



Reserve For FLX TC or PWM MDE USE By PMSPEC



RIL8111G/RIL8111H Giga LAN

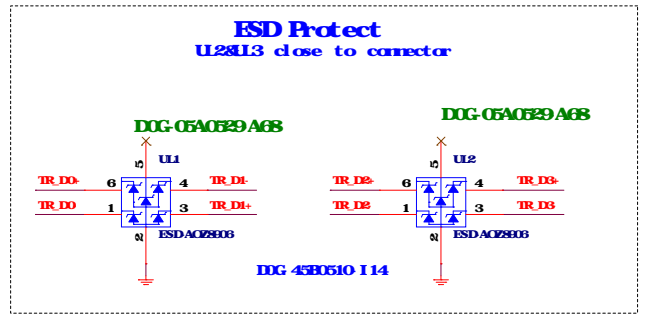
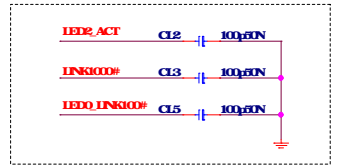
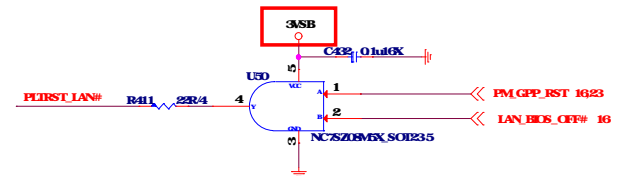
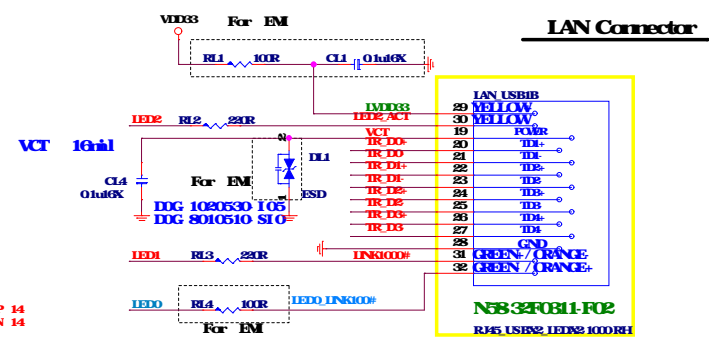


**8111G POWER Consumption**

	3.3V @ mA	mW
10 M Idle/15%	17.15/116.7	56.6/385.1
100 M Idle/15%	71.45/129.5	235.8/427.4
Giga Idle/15%	179.1/243.9	591.8/804.9
ALPS	6.41	21.15

**8111H POWER Consumption**

	3.3V @ mA	mW
10 M Idle/15%	9.9/84.69	32.67/279.48
100 M Idle/15%	48.11/92.44	158.76/305.05
Giga Idle/15%	124.5/177.57	410.85/585.98
ALPS	5.50	18.15

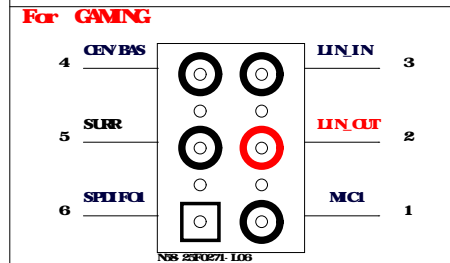
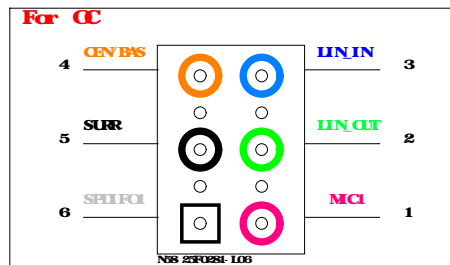
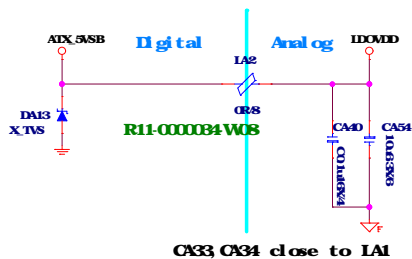
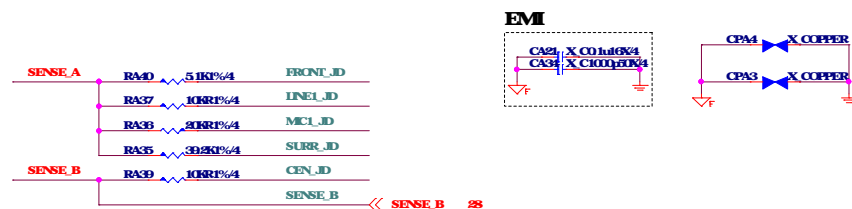
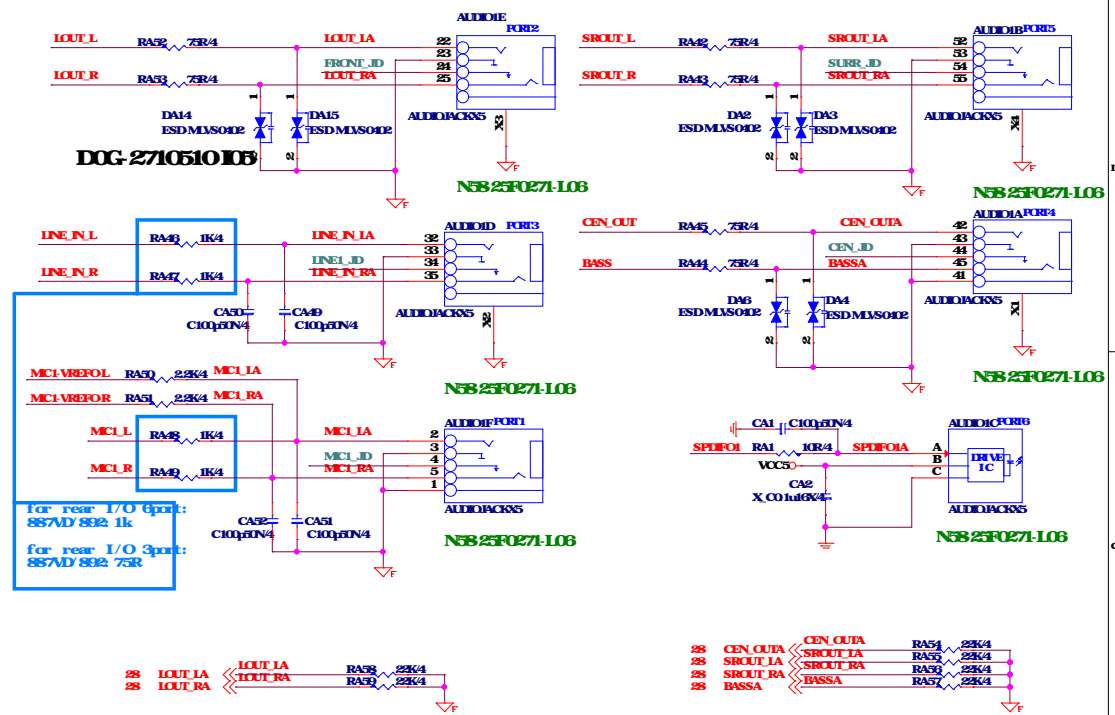


**MSI**  
MICROSTART INFL CO., LTD.  
Link to the Future

**LAN RIL8111H**

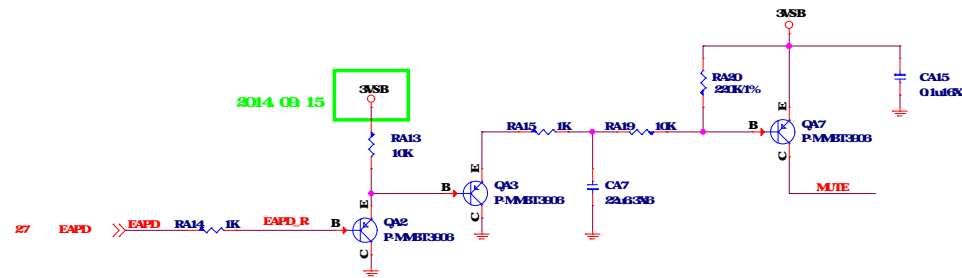
DocuNet Number: MS-7889  
Date: Wednesday, July 04, 2005  
Sheet: 20 of 28

## Follow APU power well



## Rear Line OUT De-POP circuit

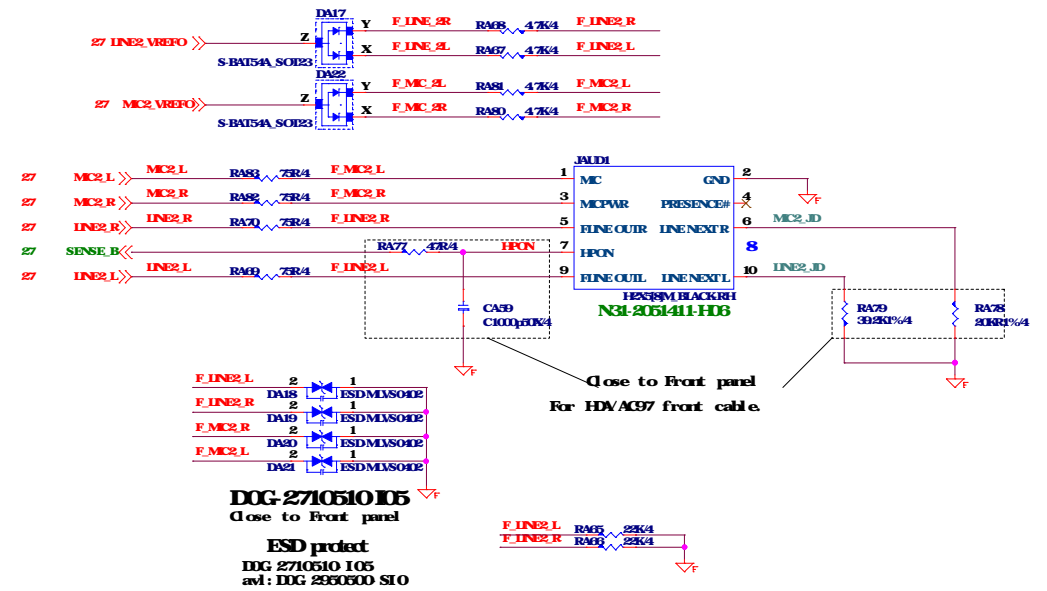
De-pop circuit for Rear Line out & Front Headphone out



## Digital

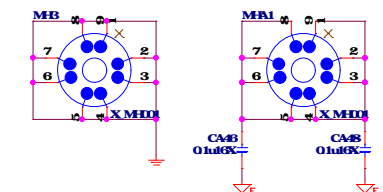


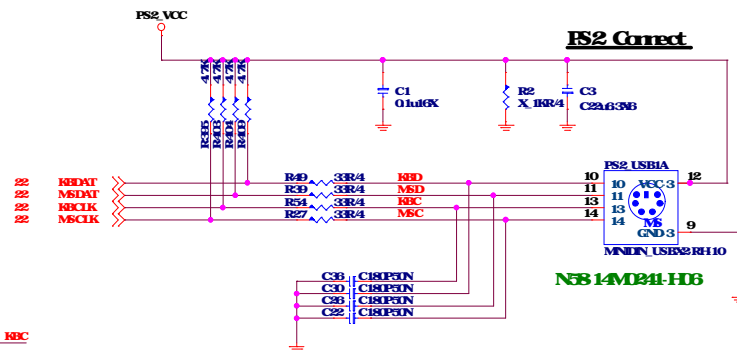
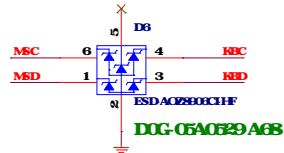
(add de-pop circuit by PMspec or customer request,  
NOTE add de-pop circuit need to change CA5, CA6, CA7, CA9 to TVS)



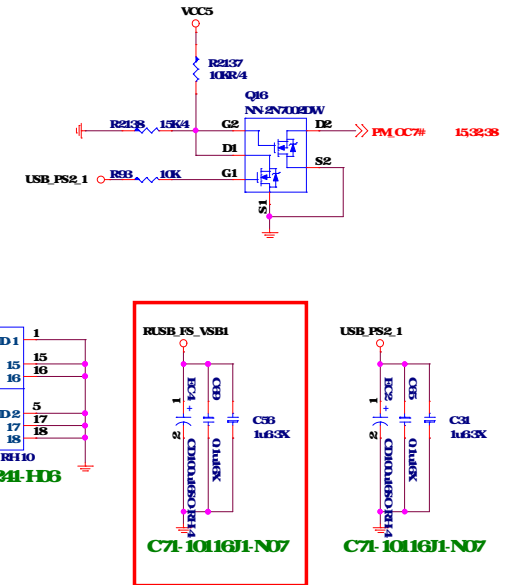
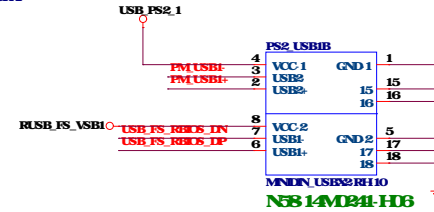
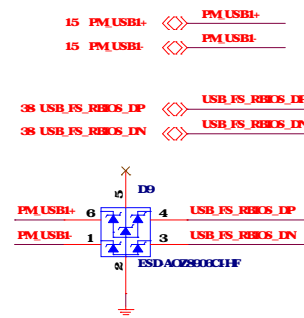
Close to Front panel  
For HDV/AG97 front cable

DOG-2710510 I05  
Close to Front panel  
ESD protect  
DOG-2710510 I05  
av1: DOG-2950500 SI0

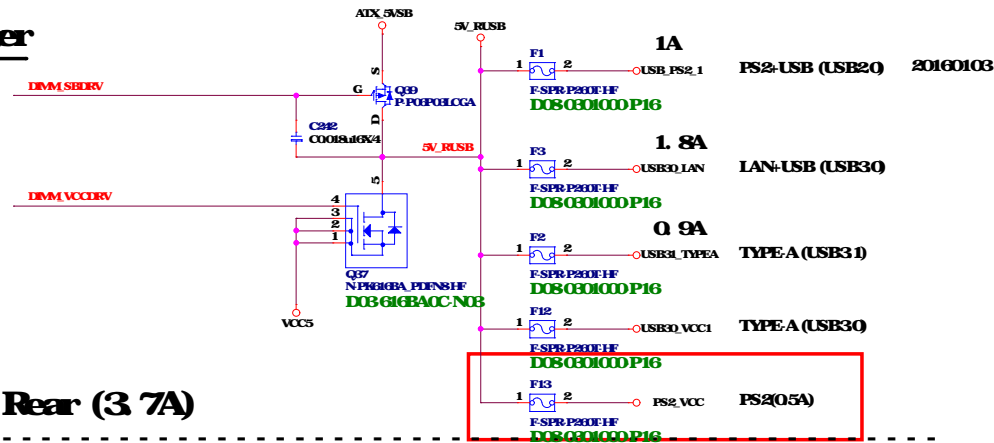


**PS2+USB**TVS P/N  
DOG 45B0510 I 14

layout note  
C21 must close to TVS pin5  
TVS must near KB\_M1 connector and route without branch  
Varistor must close to TVS and route without branch

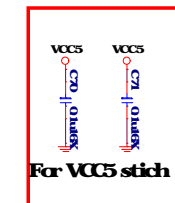


## USB Power



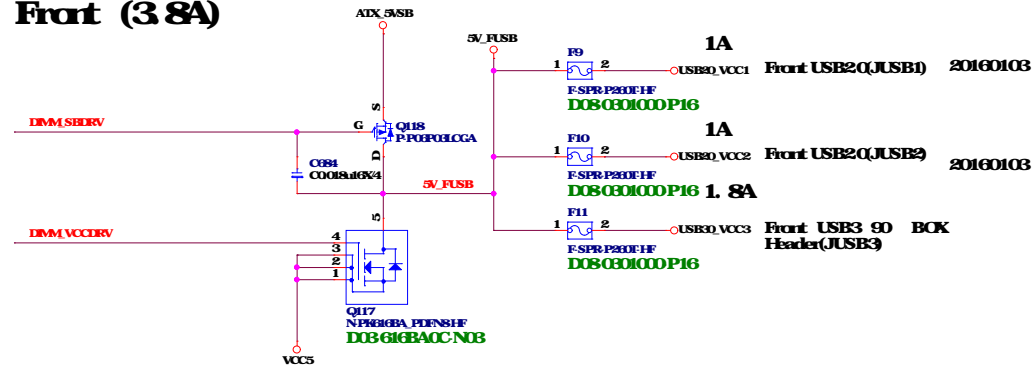
40 DIMM\_VCCDRV << DIMM\_VCCDRV

3840 DIMM\_SBDRV << DIMM\_SBDRV



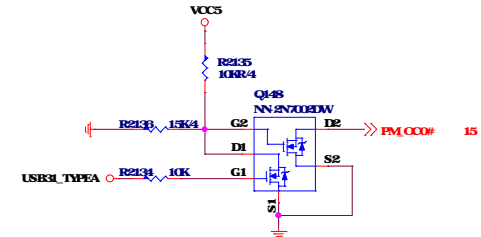
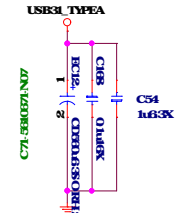
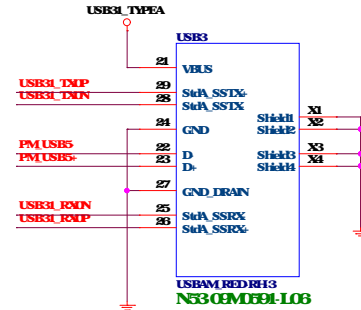
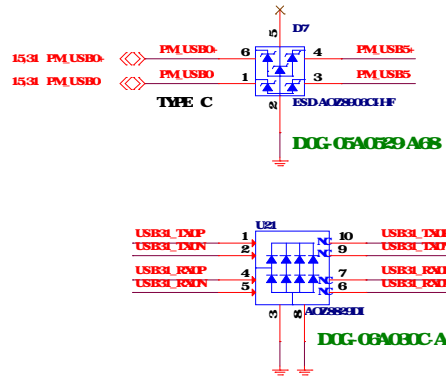
**For VOC5 stich**

### Rear (3 7A)

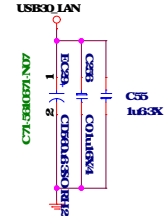
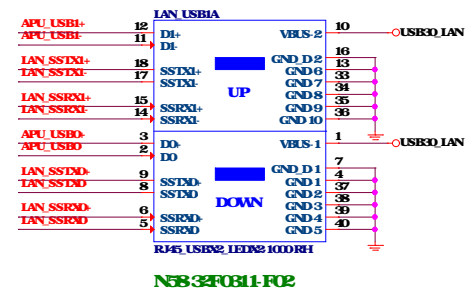
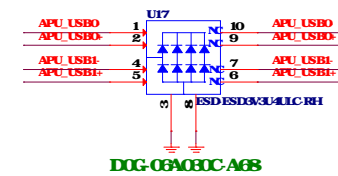
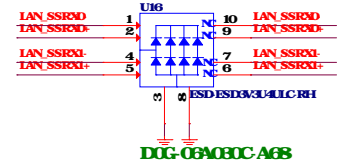
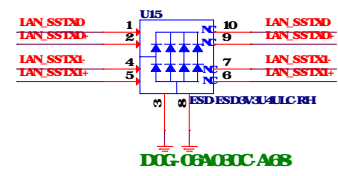
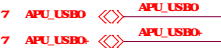
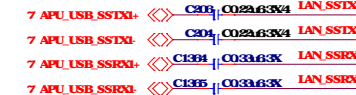
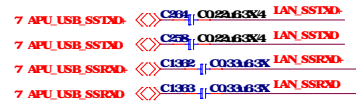
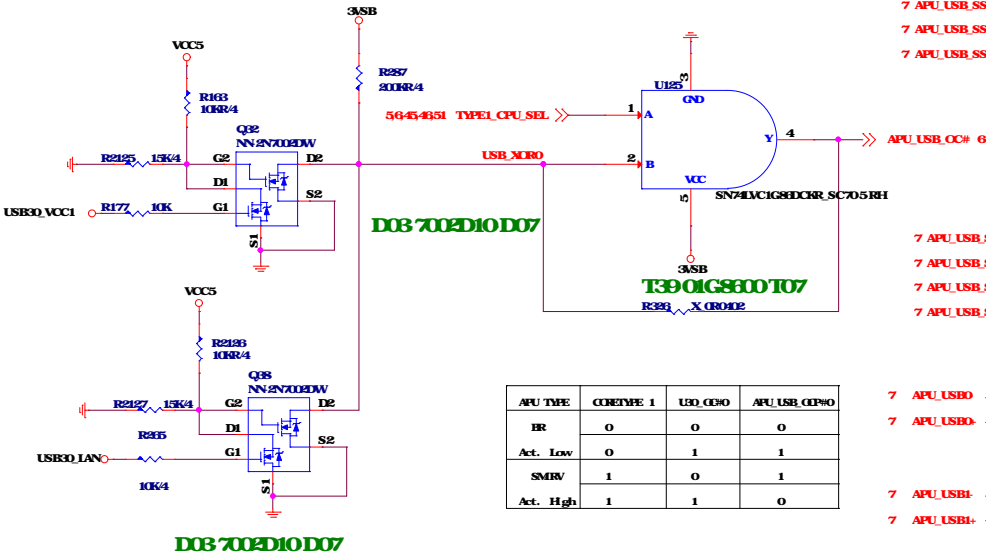
**Front (3 8A)**



# TYPE A USB 3 1



# LAN+USB (USB3 0)

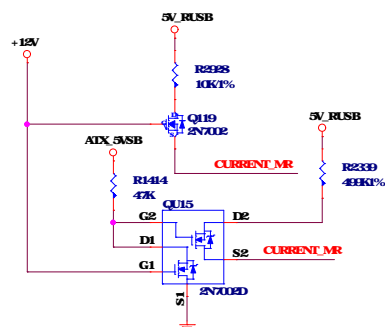
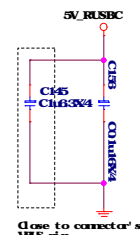
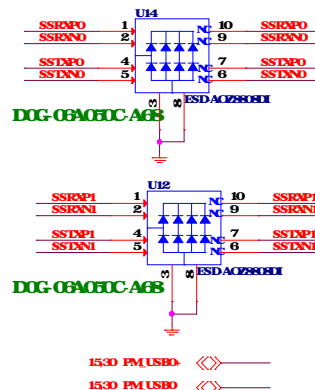
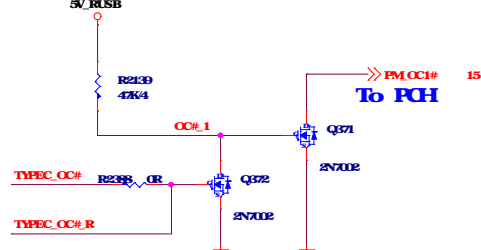


APU TYPE	CORETYPE	1	USB_OC0	APU_USB_OC#0
BR	0	0	0	0
Act. Low	0	1	1	1
SMBV	1	0	1	1
Act. High	1	1	1	0

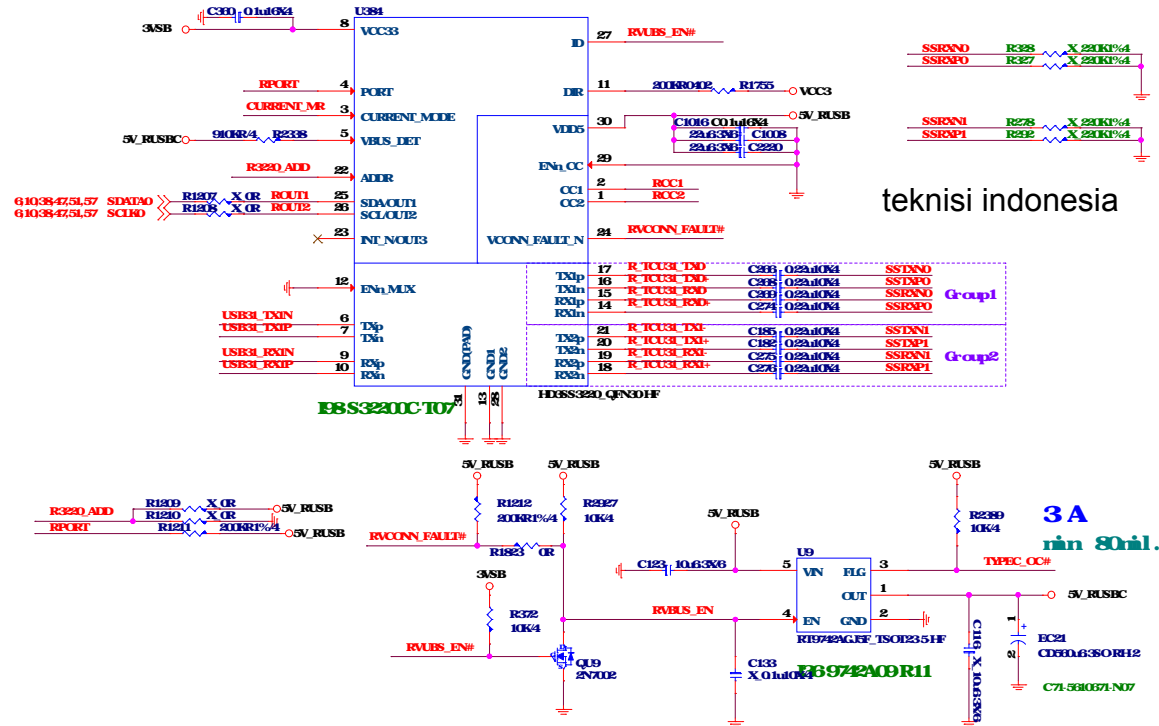
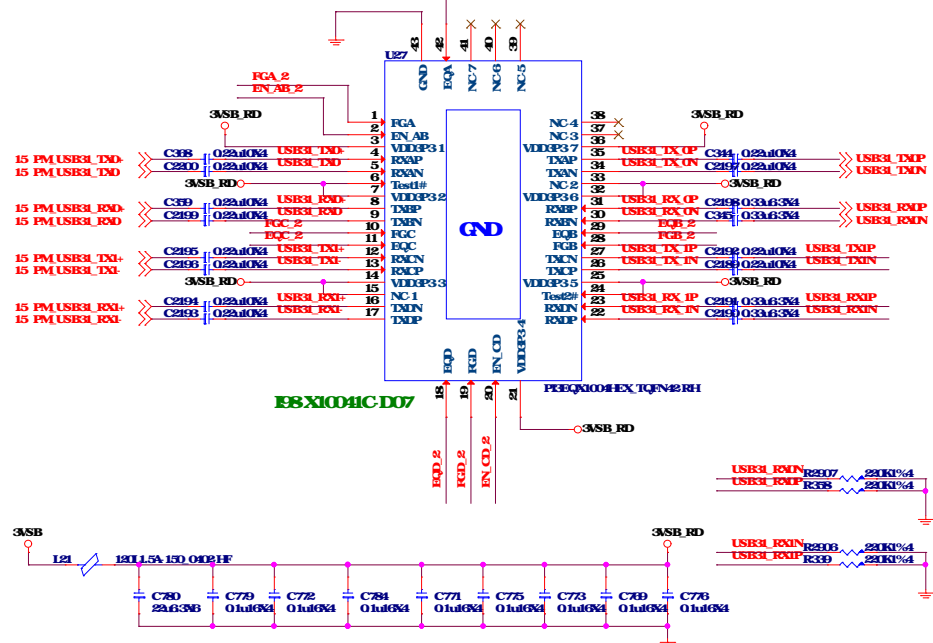
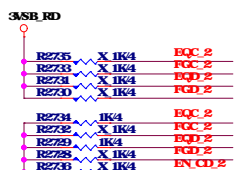
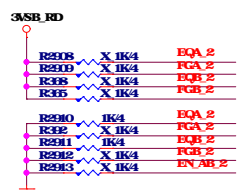
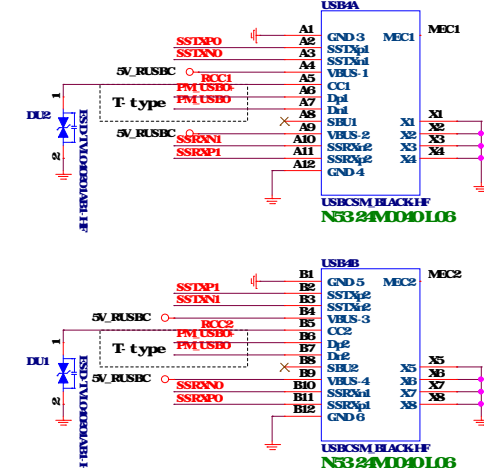
**5V@3A**

## Current Mode

L - Default for 900mA  
M- Mid (500K) for 1.5A  
H- High (10K) for 3A

**VBLS CC#**

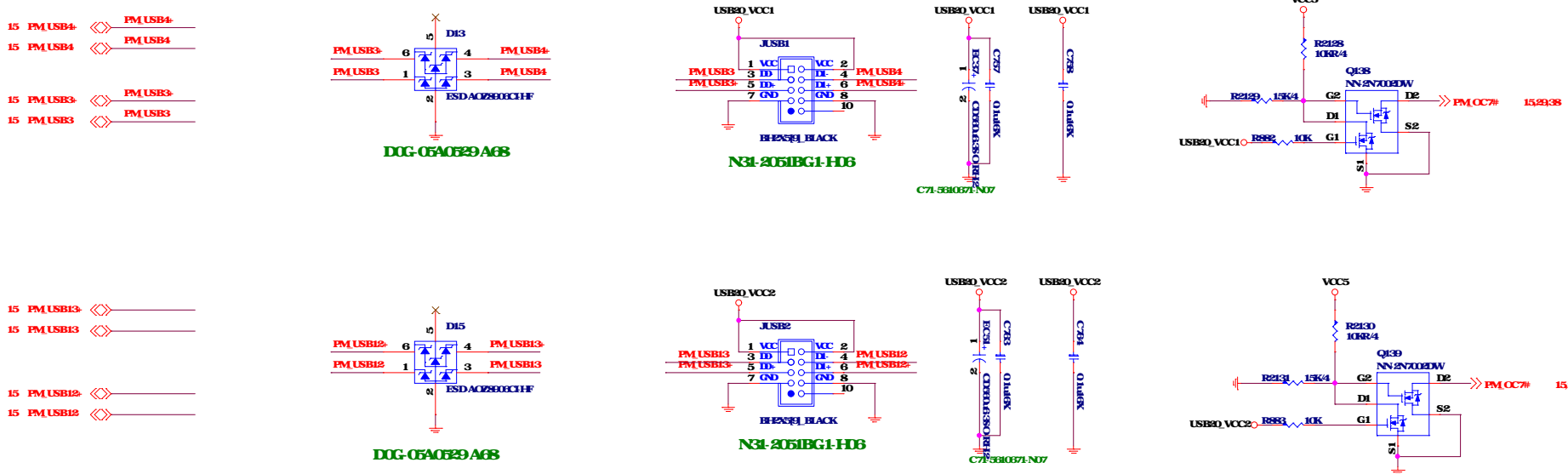
Close to connector's  
WFE-1-



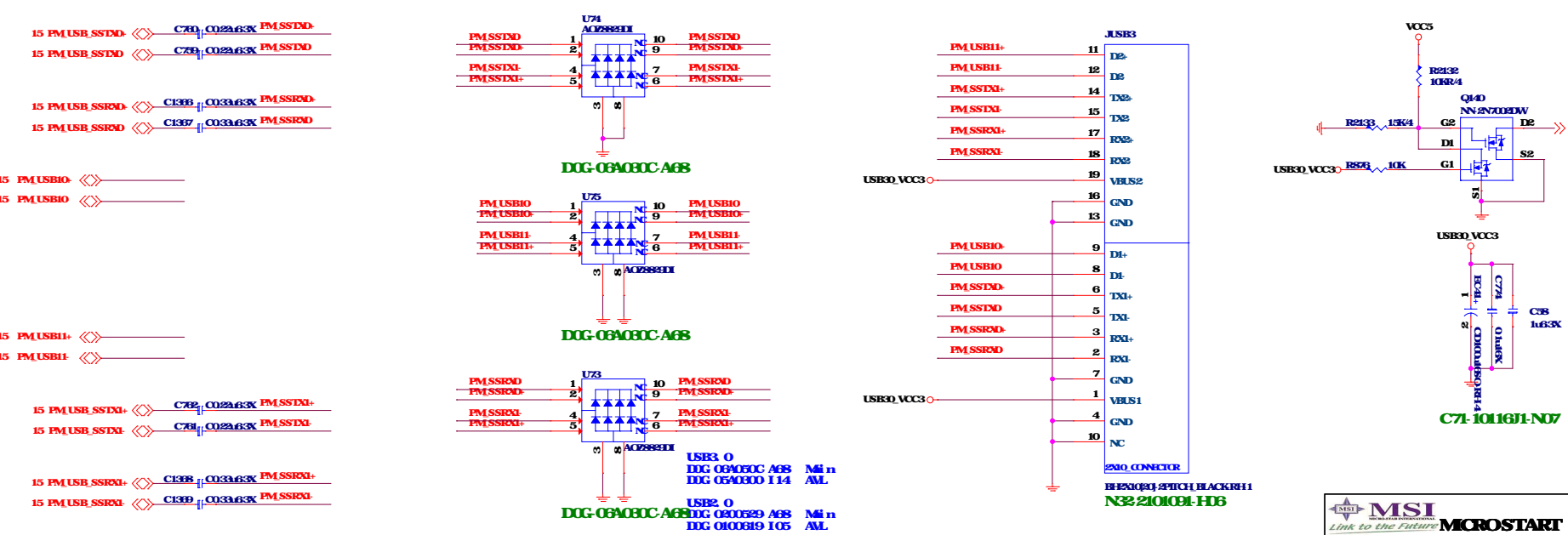
teknisi indonesia

**3 A**  
min 80ml.

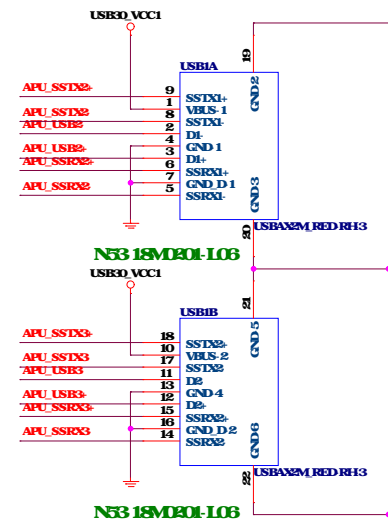
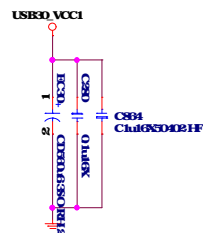
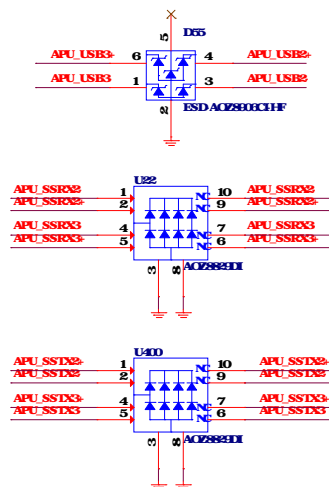
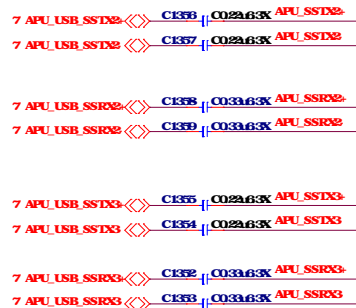
Front USB20



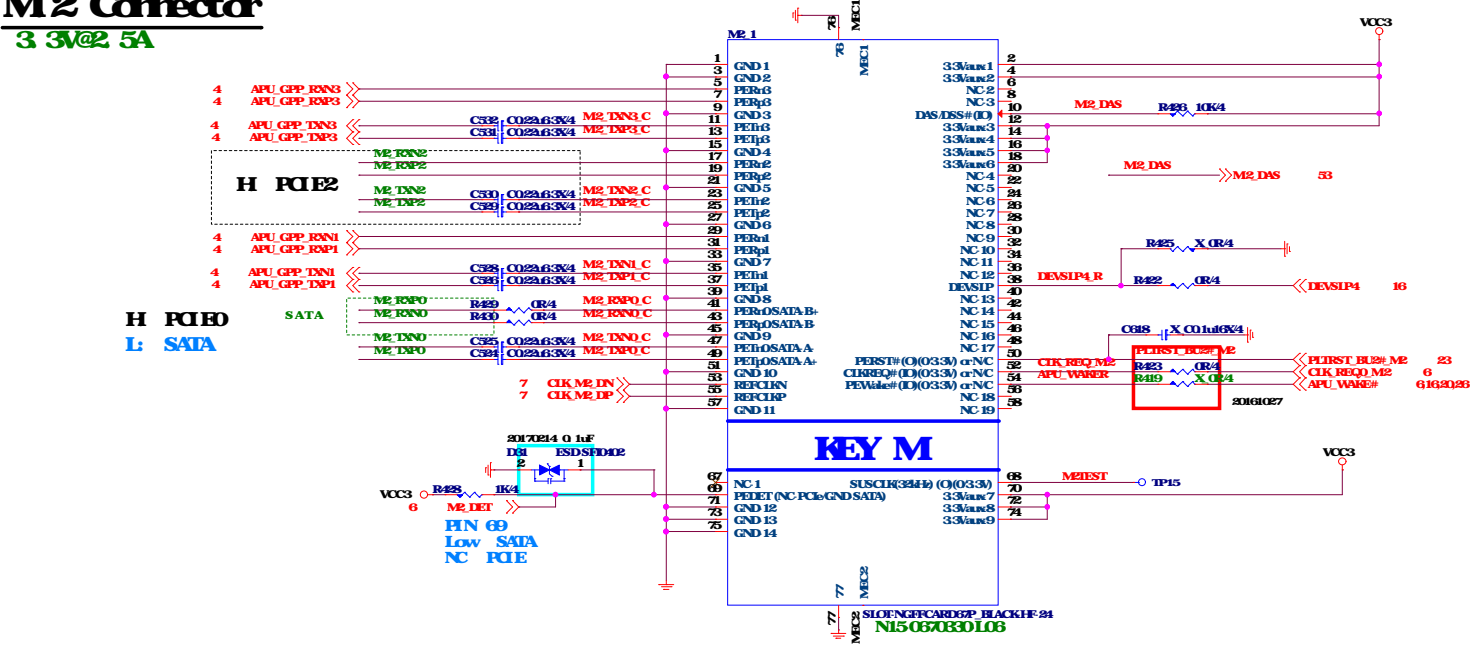
Front USB31 GEN1



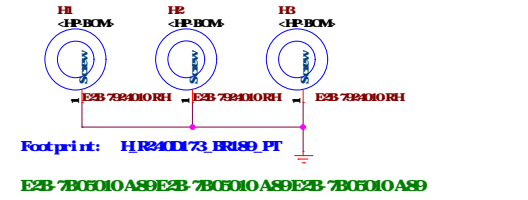
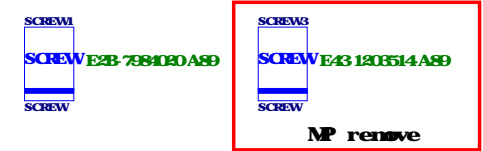
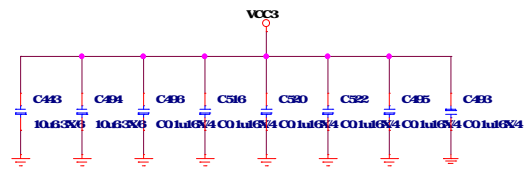
# USB3 0



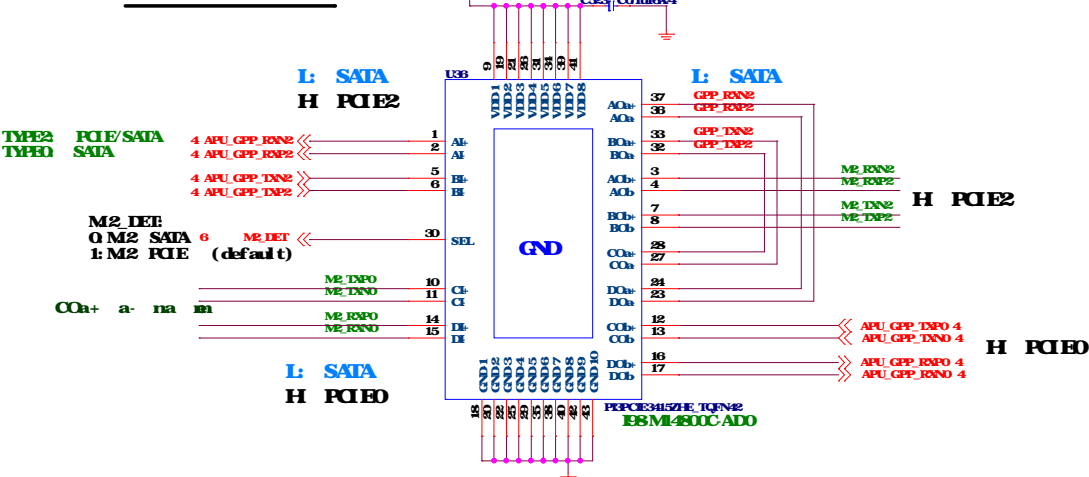
M2 Connector  
3 3V@2 5A



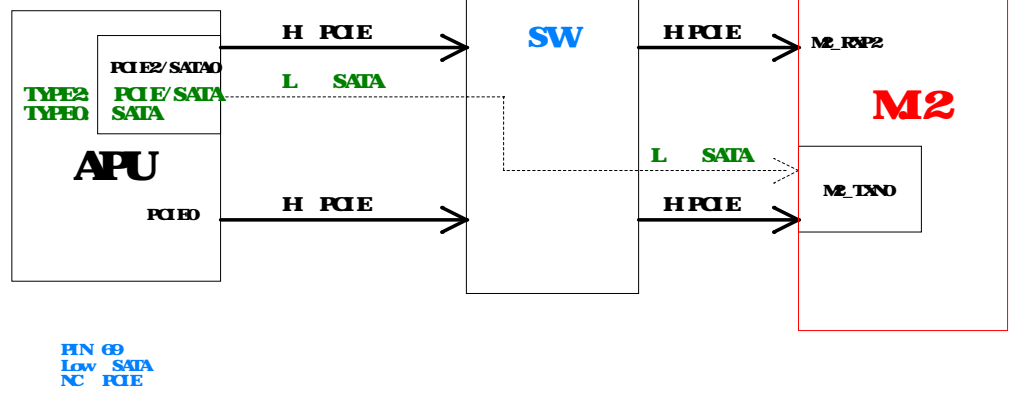
3 3V@2 5A



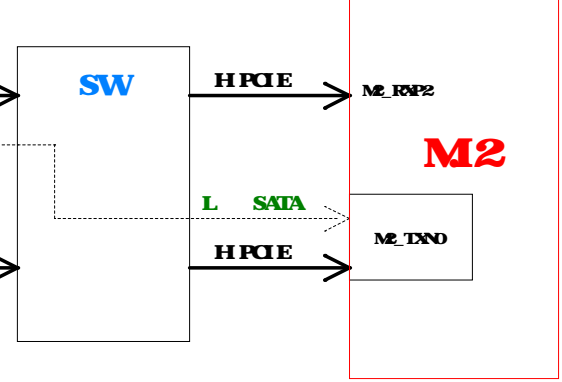
M2 Switch



HWDefault  
M2 Insert

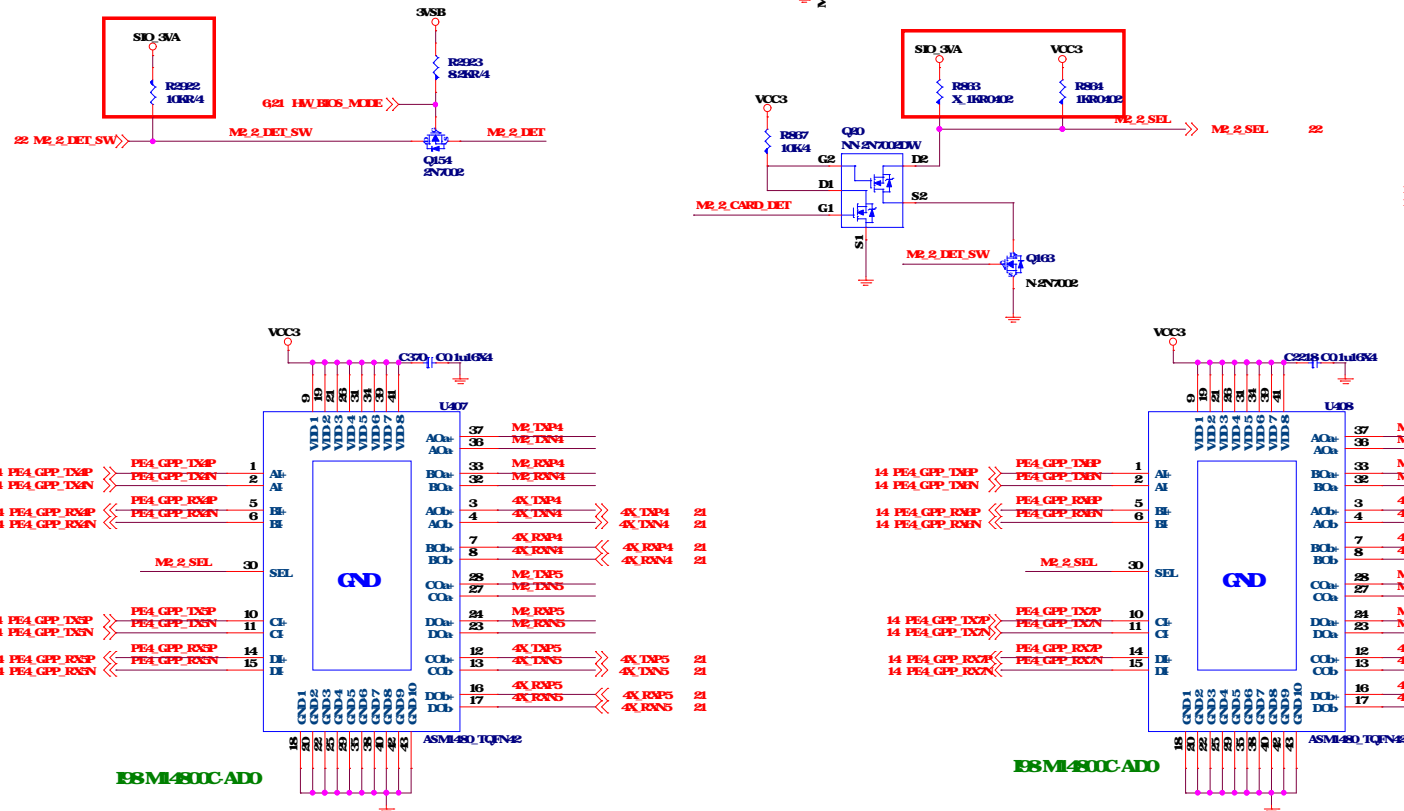
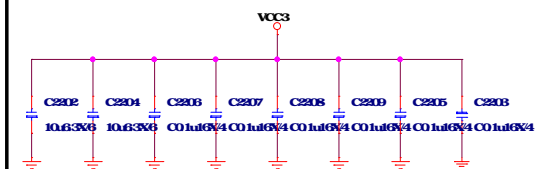


SW  
HM2 PCIe  
L: M2 SATA



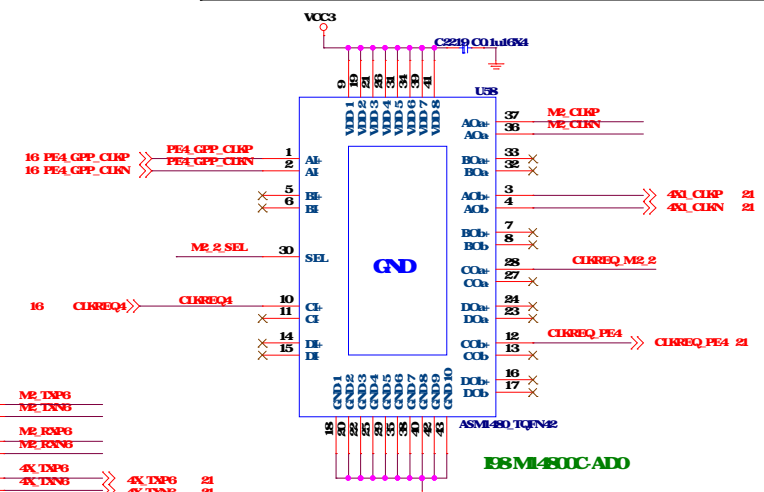


**3 3V@2 5A**

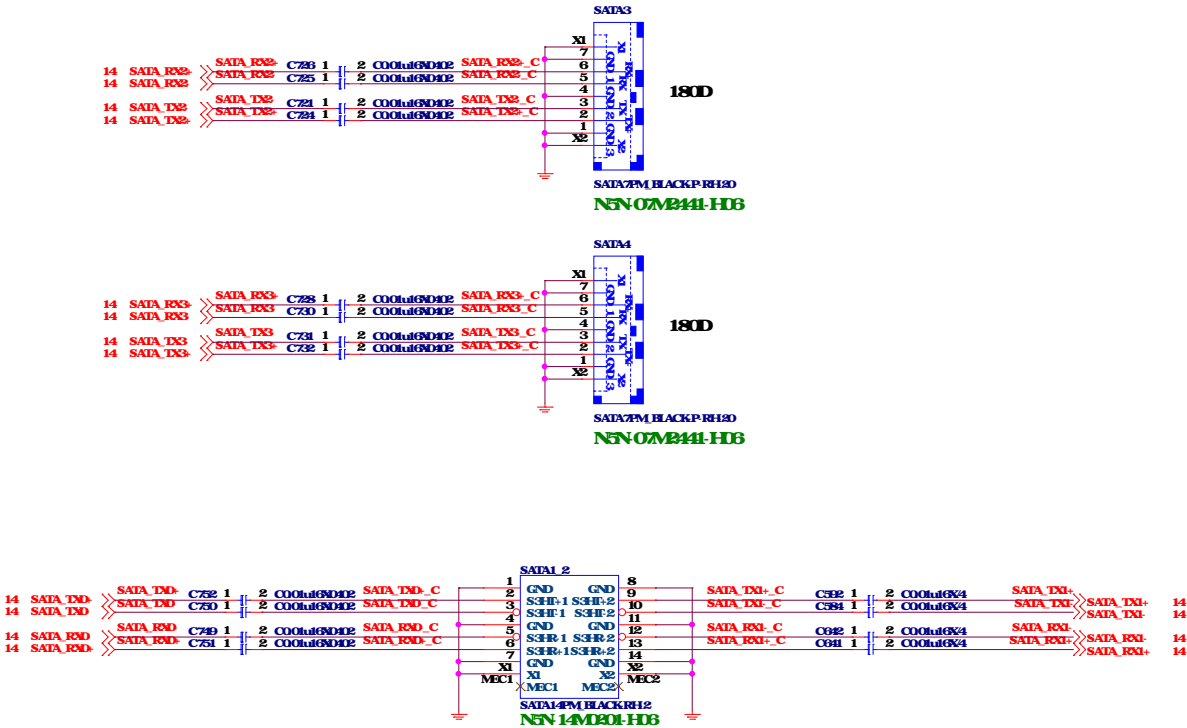
**98M14800C-ADO**

Footprint: H\_R240D173\_BR189\_PT

E2B-7B05010A89E2B-7B05010A89E2B-7B05010A89

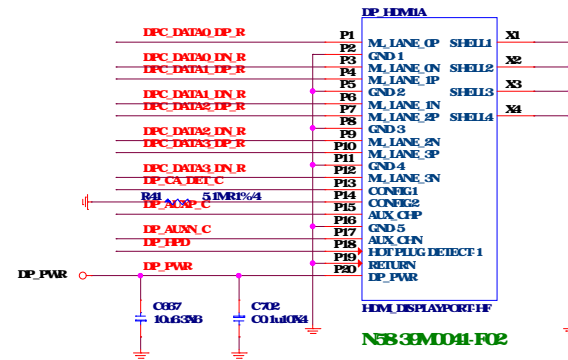
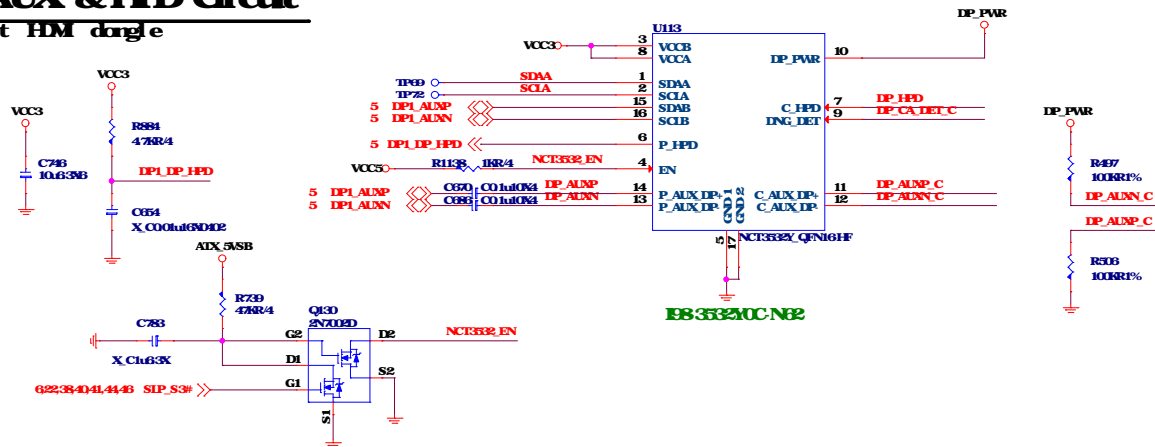
**E98M4800C-ADO**

SATA Connector



## DP AUX & HD Circuit

### Support HDMI dongle



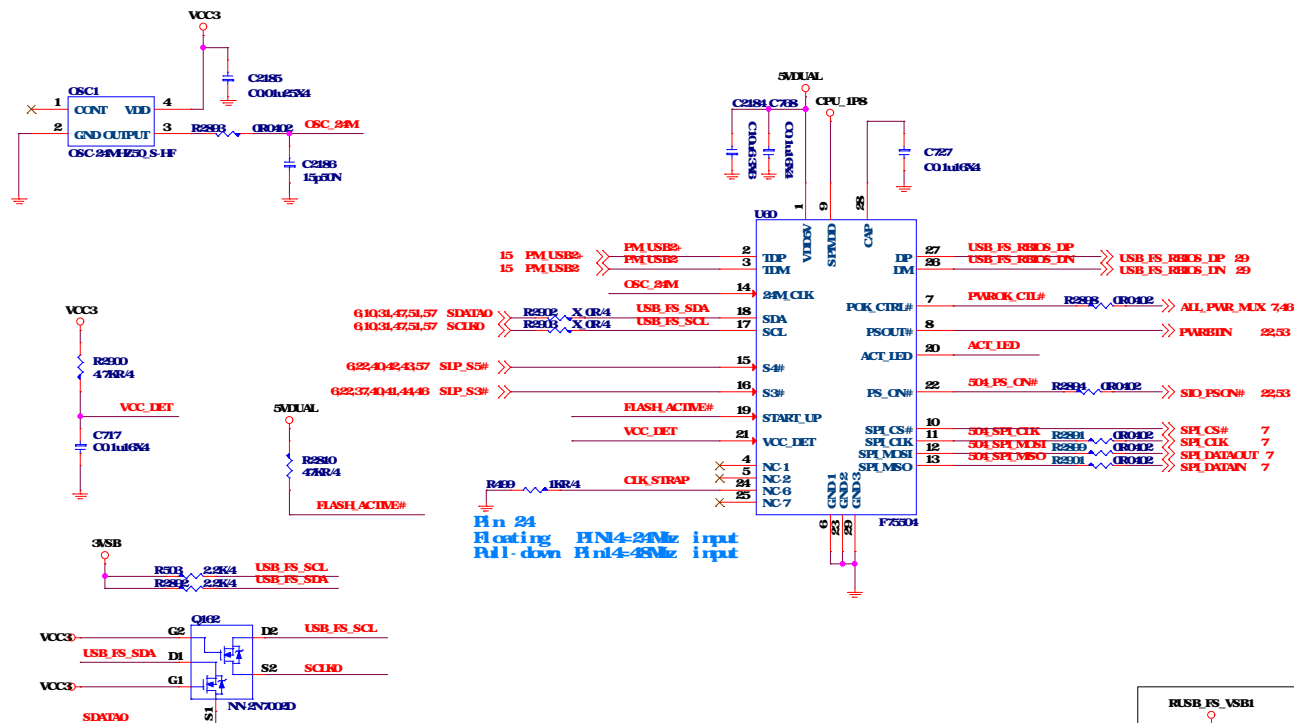
The first diagram shows the DOG-06A0829A68 component. It has a 4x4 pin grid. The top row is connected to DP\_ALN\_P.C (pin 6), DP\_HPD (pin 4), and DP\_ALN\_N.C (pin 1). The right side has connections to DP\_HPD (pin 4), DP\_ALN\_N.C (pin 3), and ESDA02803CH.F (pin 2). The bottom row is connected to ground (pin 0). The component is labeled DOG-06A0829A68.

The second diagram shows the DOG-06A080CA68 component. It has a 4x4 pin grid. The top row is connected to DFC\_DATA2.DP.R (pin 1), DFC\_DATA2.DN.R (pin 2), DFC\_DATA3.DP.R (pin 4), and DFC\_DATA3.DN.R (pin 5). The right side has connections to DFC\_DATA2.DP.R (pin 10), DFC\_DATA2.DN.R (pin 9), DFC\_DATA3.DP.R (pin 7), and DFC\_DATA3.DN.R (pin 6). The bottom row is connected to ground (pin 0). The component is labeled DOG-06A080CA68.

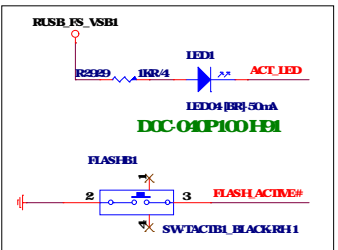
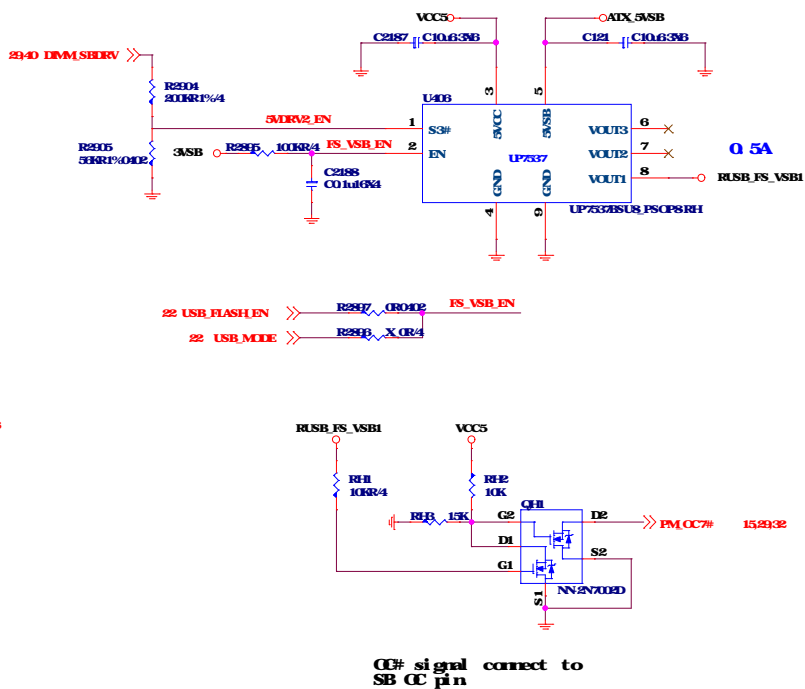
The third diagram shows the DOG-06A080CA68 component. It has a 4x4 pin grid. The top row is connected to DFC\_DATA2.DN.R (pin 1), DFC\_DATA2.DP.R (pin 2), DFC\_DATA0.DN.R (pin 4), and DFC\_DATA0.DP.R (pin 5). The right side has connections to DFC\_DATA2.DN.R (pin 10), DFC\_DATA2.DP.R (pin 9), DFC\_DATA0.DN.R (pin 7), and DFC\_DATA0.DP.R (pin 6). The bottom row is connected to ground (pin 0). The component is labeled DOG-06A080CA68.

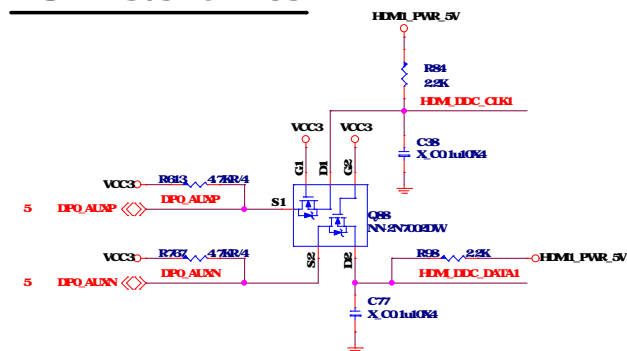
# USB Flash BIOS

Hist USB connector

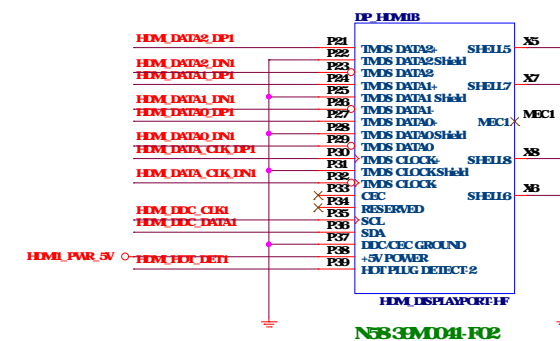


## REAR Flash BIOS USB

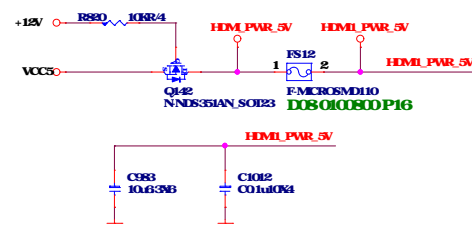
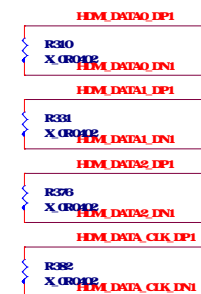
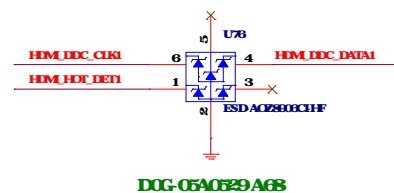
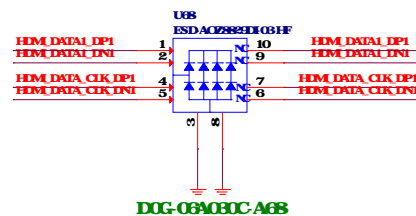


**For HDM 1.4**

## Connector



## Connector Power

**For EM**

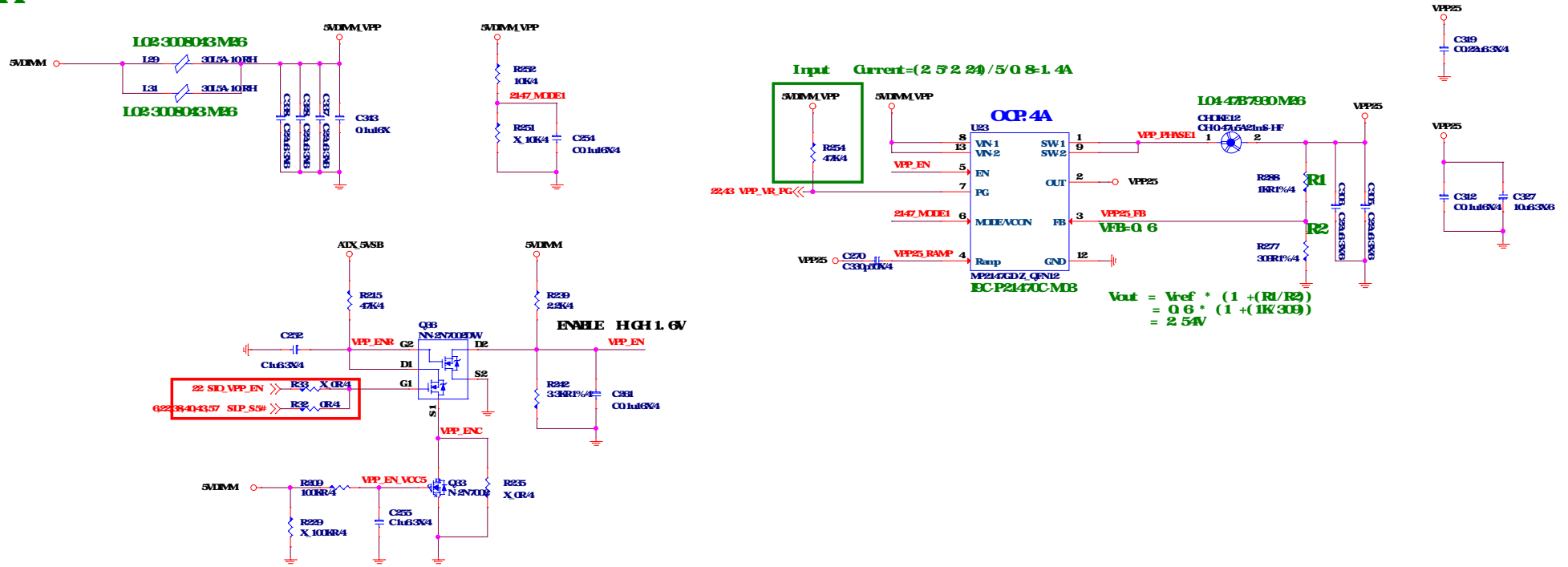






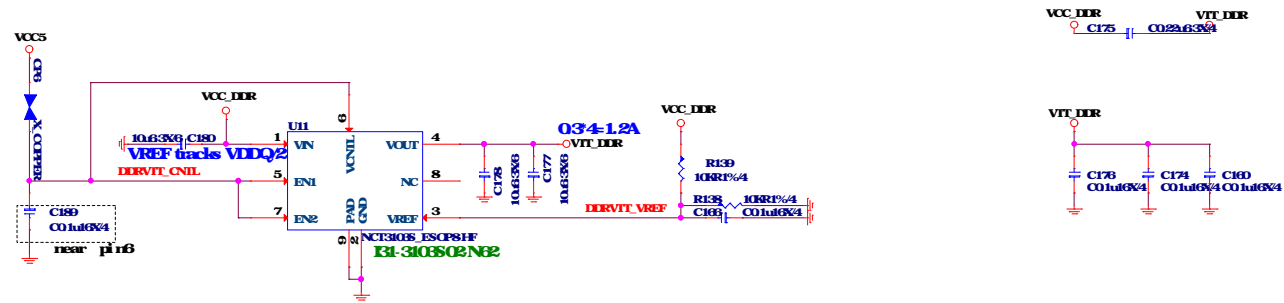
# 4DIMM: VPP25

2.5V@2.24A

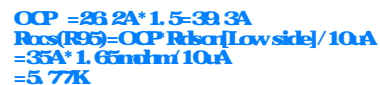
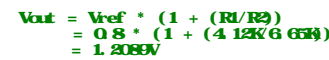


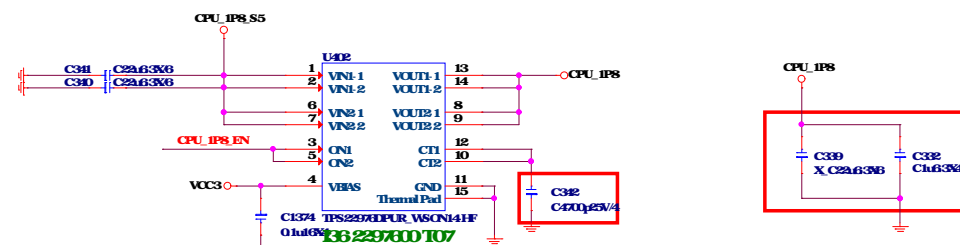
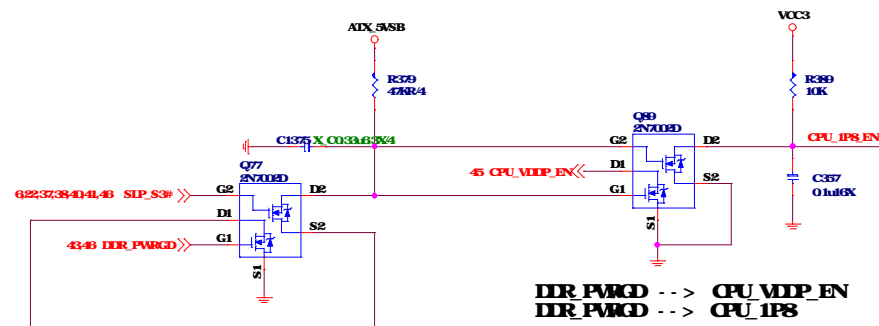
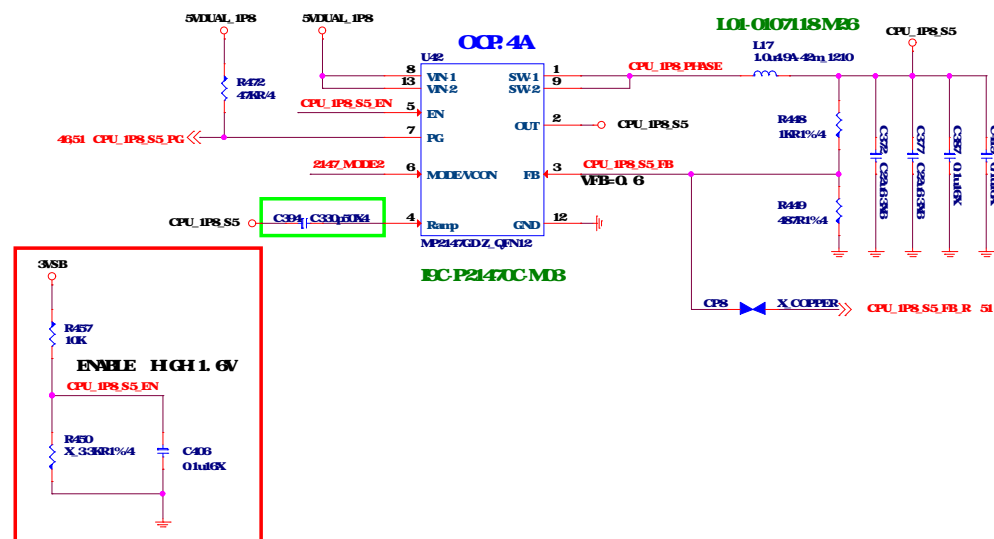
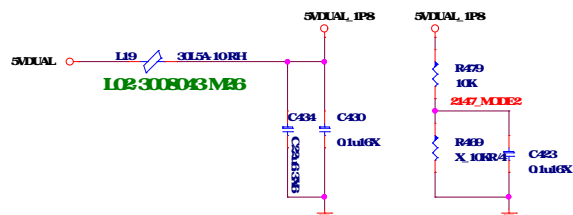
## DDR VIT Power

To CPU Copper trace width > 250mils, H11 island behind DIMM > 400mils.



**15.5A FOR CPU**  
**9.5A FOR 4DIMM**  
**1.2A FOR DDR VTT**



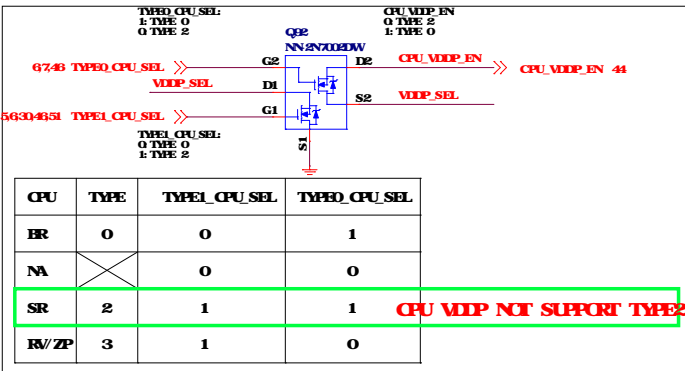
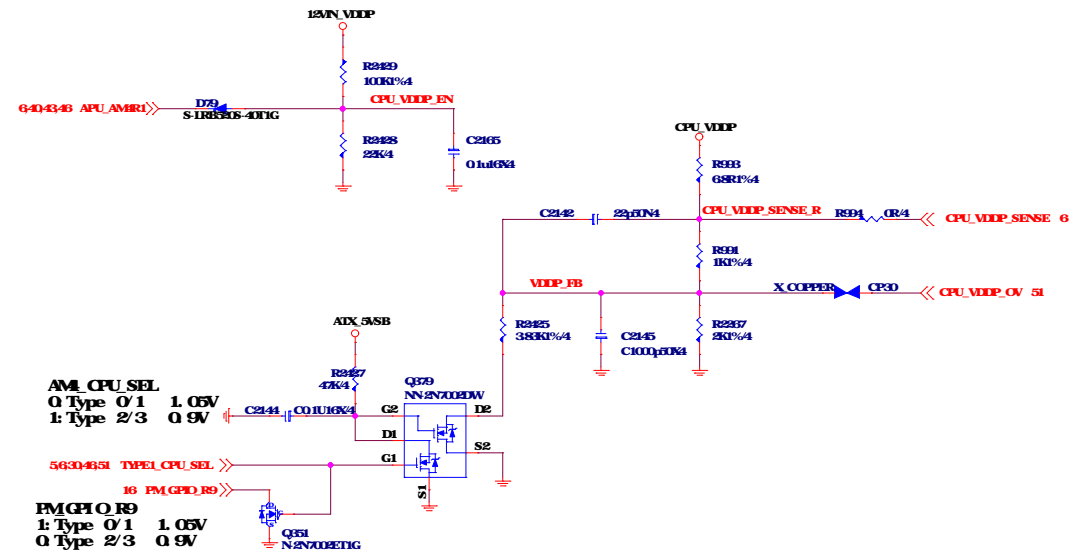
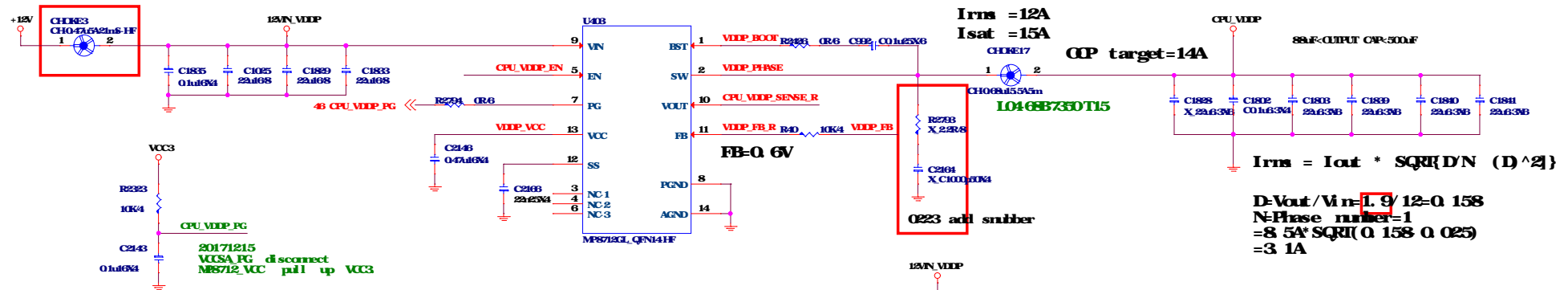
$$0.5A + 2.0A + 0.9A = 3.4A$$


**Adjustable Rise Time**  
 $SR = 0.42 / CT + 66$   
 SR is the slew rate in ( s/V)  
 CT is constant value on CT pin (in pF)  
 The units for the constant 66 is in  
 ( s/V)

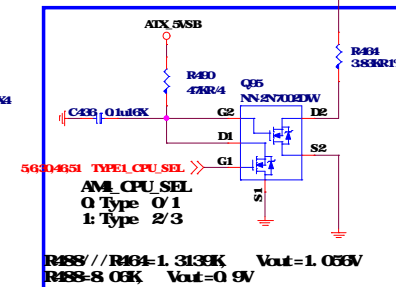
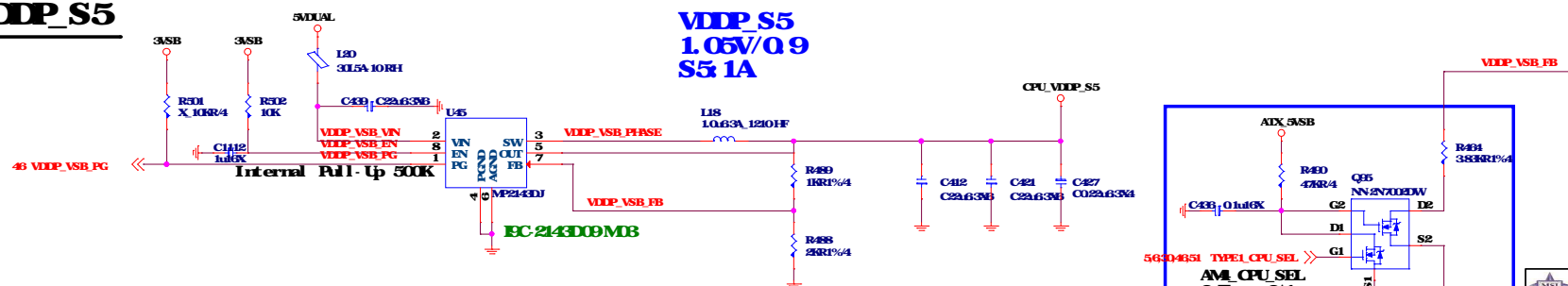


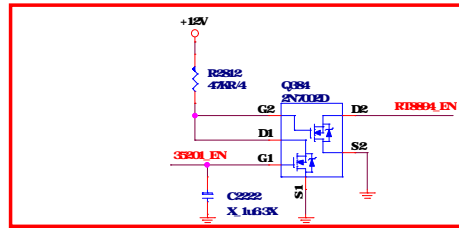
**CPU\_VDDP\_S0**

**1.05V/0.9  
SQ8.5A**

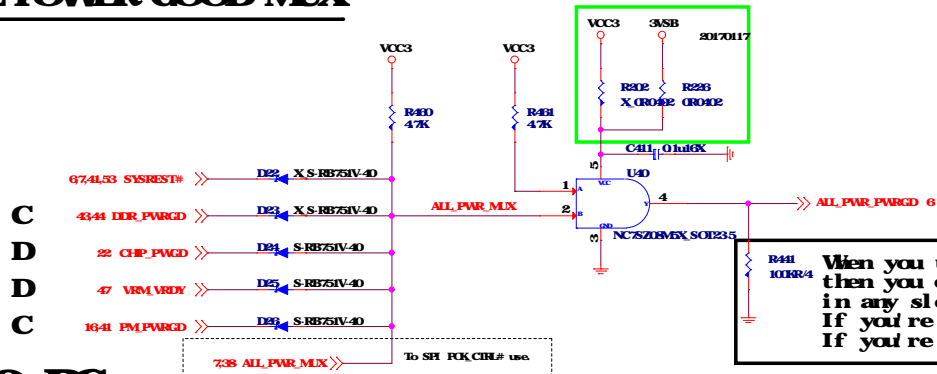
**CPU\_VDDP\_S5**

**VDDP\_S5**  
**1.05V/0.9**  
**S5: 1A**

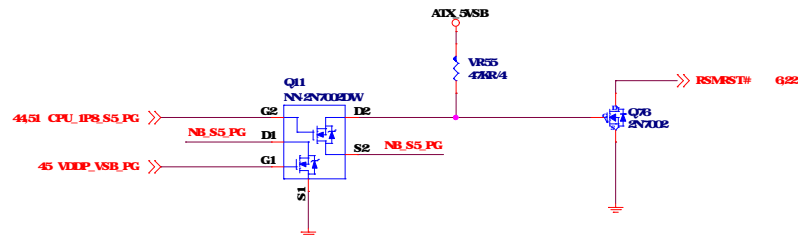




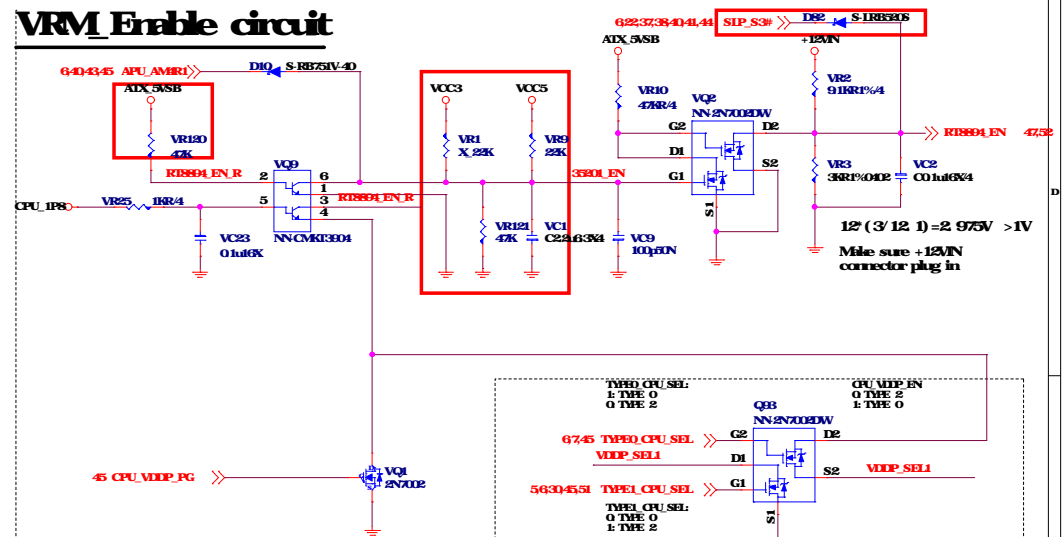
## ALL POWER GOOD MUX



S0 PG  
S5 PG

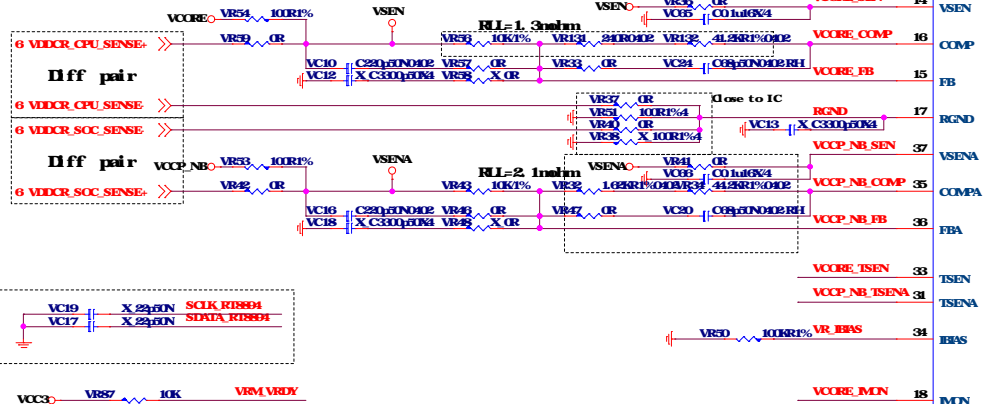
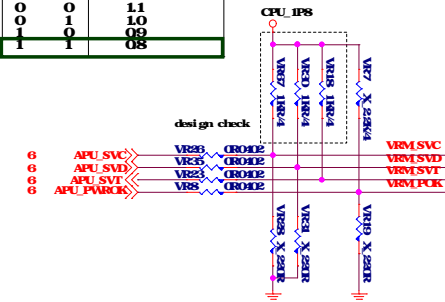


## VRM Enable circuit

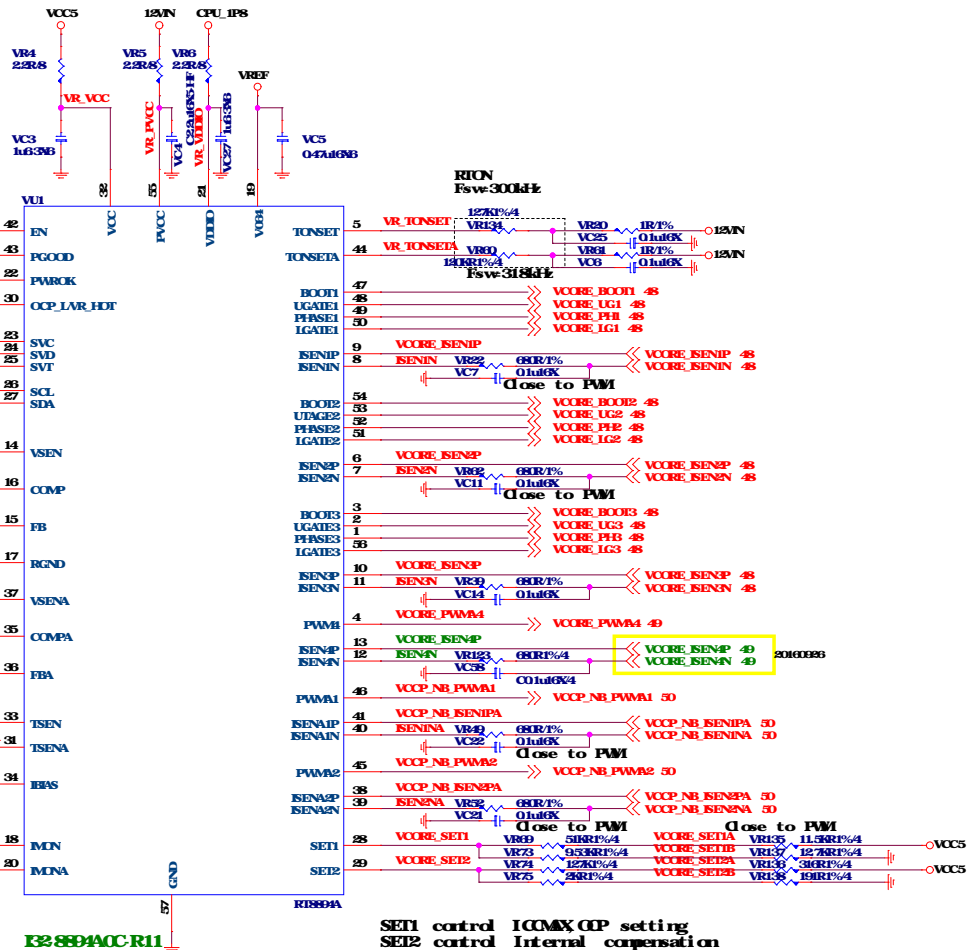
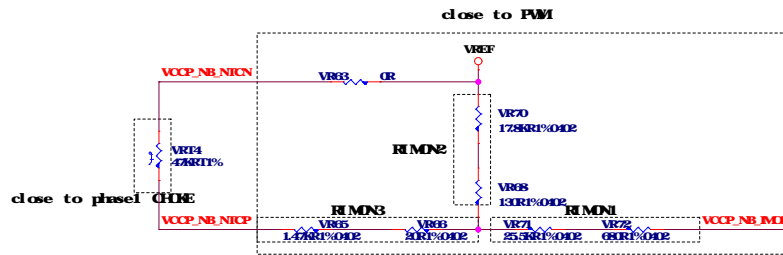
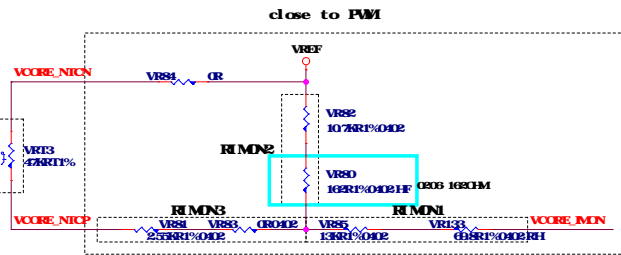
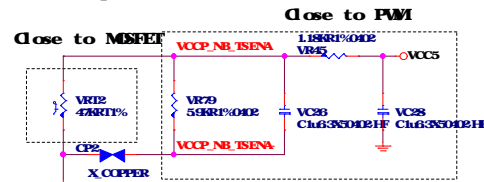
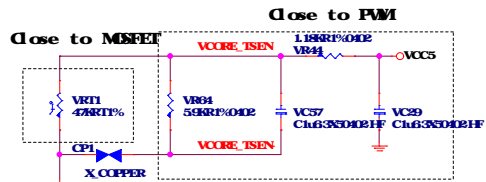


CPU VDDP NOT SUPPORT TYPE2

CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
R/ZP	3	1	0



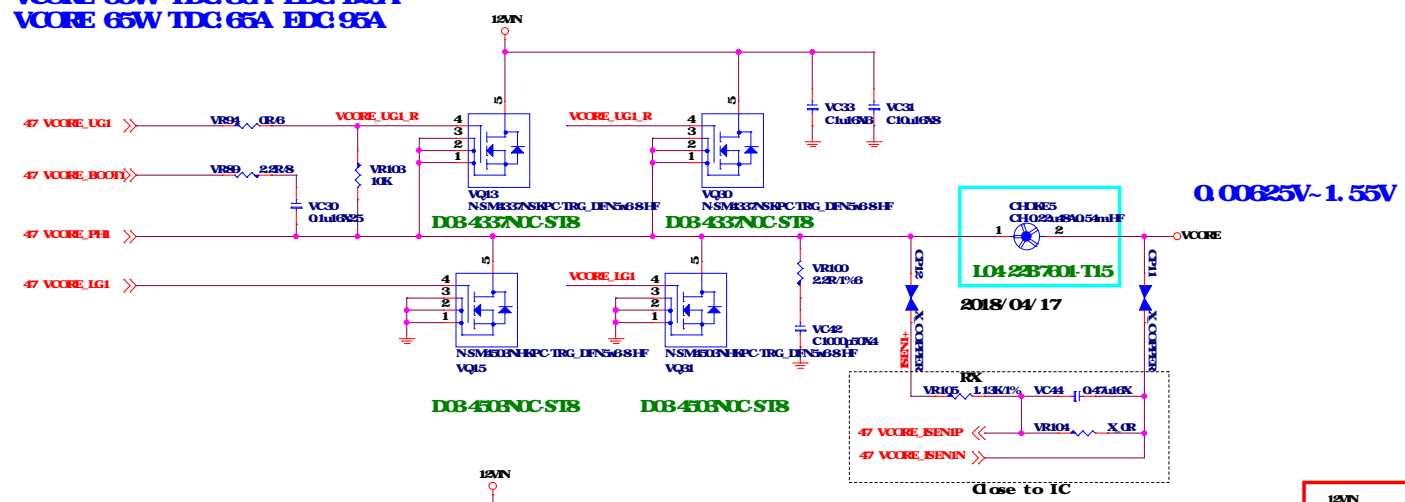
VR\_HD# pull low when T>110  
VR\_HD# pull high when T drop to 90  
Choose VRHT\_LOW=51%VCC and VRHT\_HIS=5%VCC



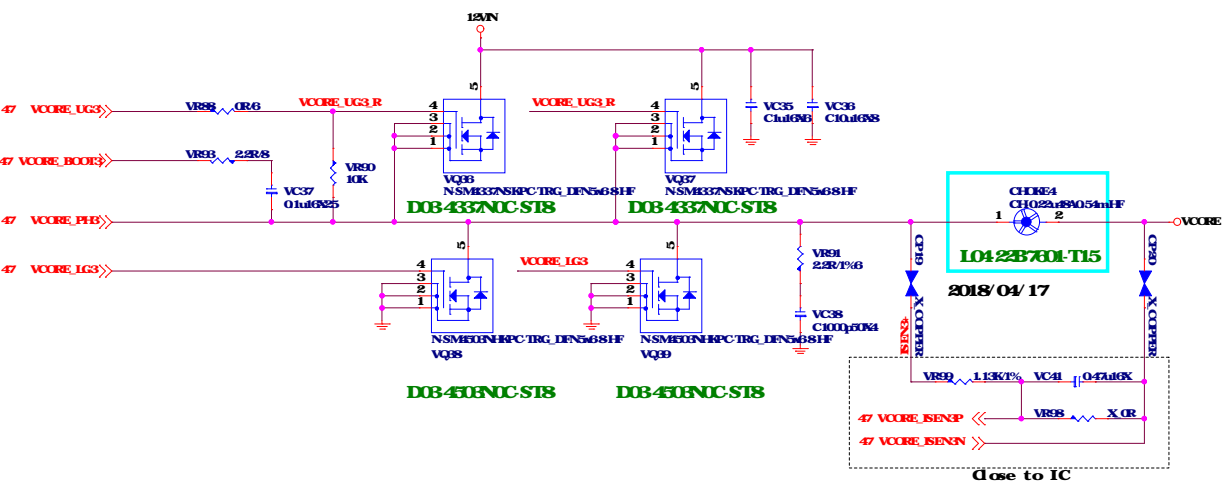
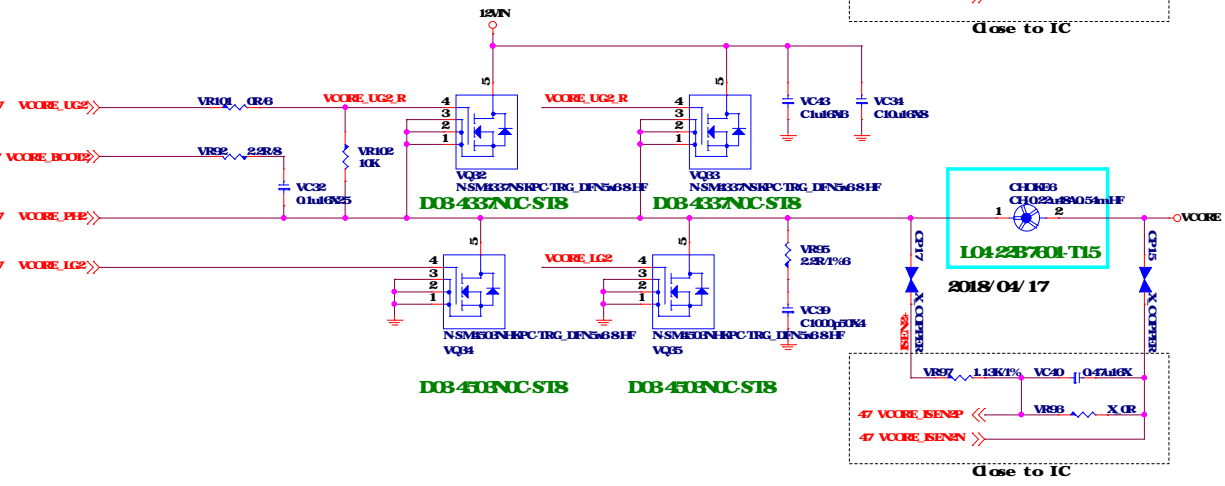
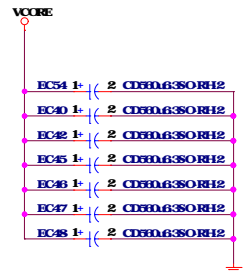
SE1	control	ICCMX_OCP setting
SE2	control	Internal compensation

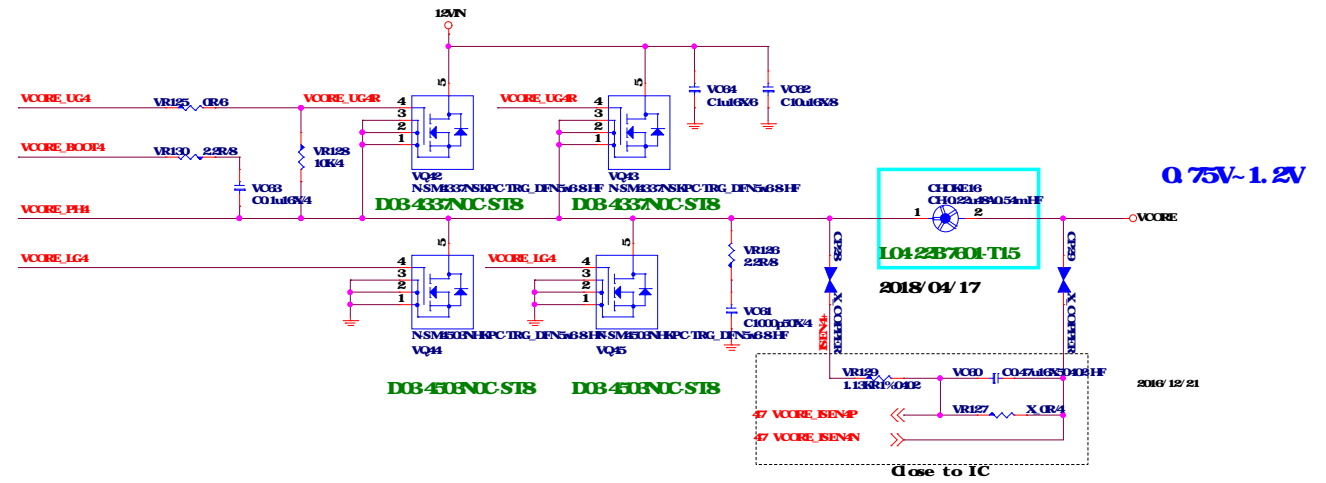
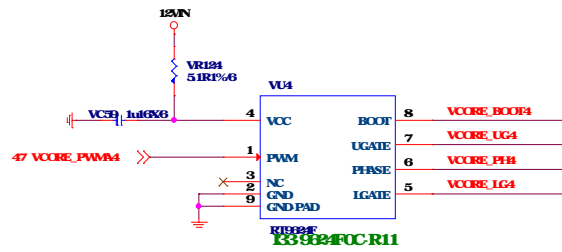
VORE IccMAX 125A =>OCP=>200A  
VCC\_NB IccMAX 75A =>OCP=> 90A

V<sub>CO</sub>RE 95W TDC 80A EDC 125A  
V<sub>CO</sub>RE 65W TDC 65A EDC 95A

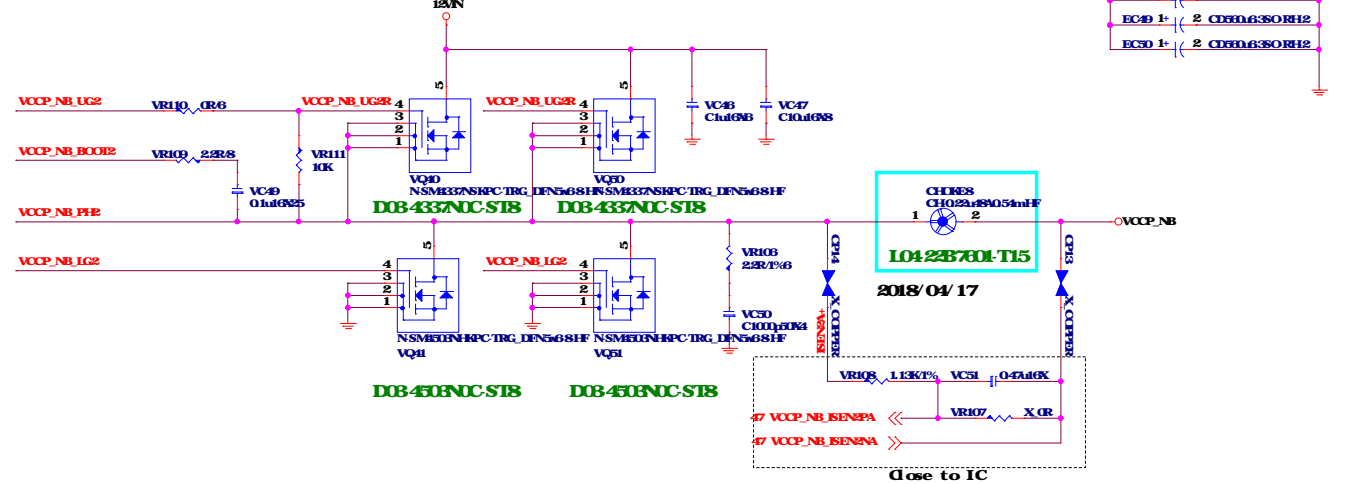
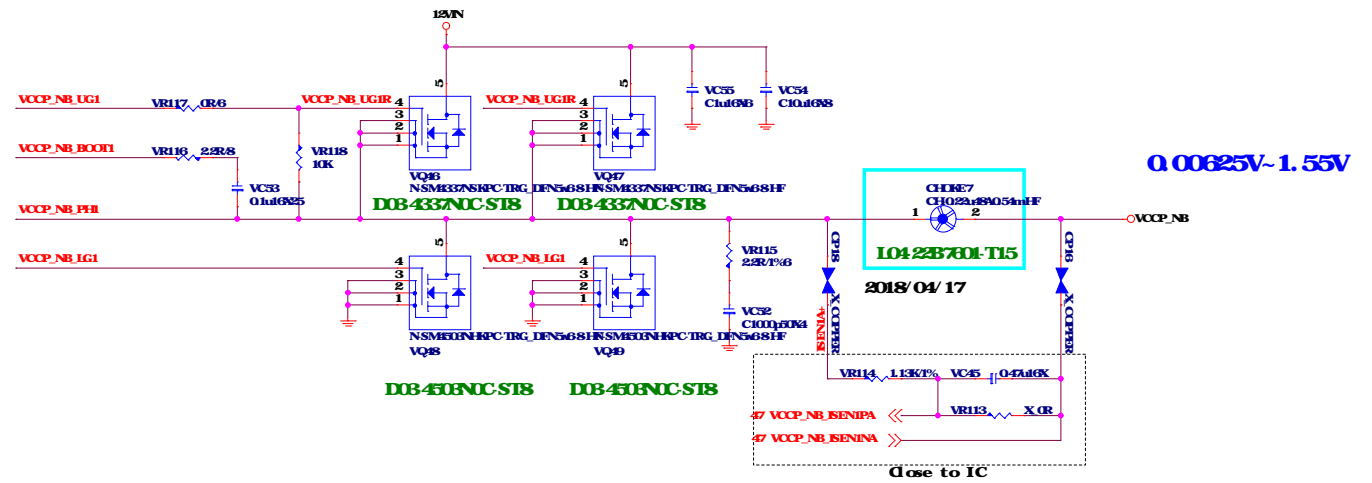
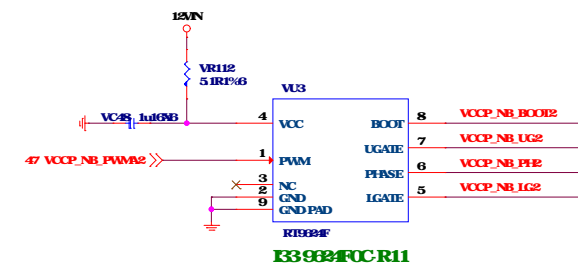
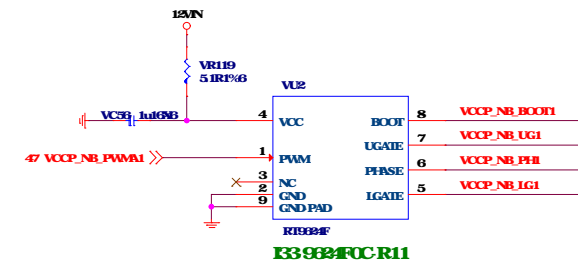


12V IN  
C383  
0.1uF25V6  
For lower switching noise





VCCP\_NB 95W TDC 50A EDC 75A  
VCCP\_NB 65W TDC 50A EDC 75A





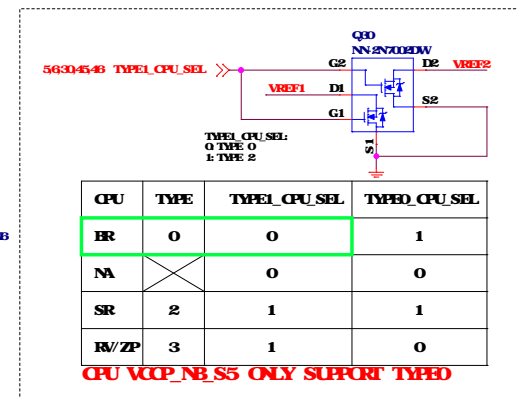
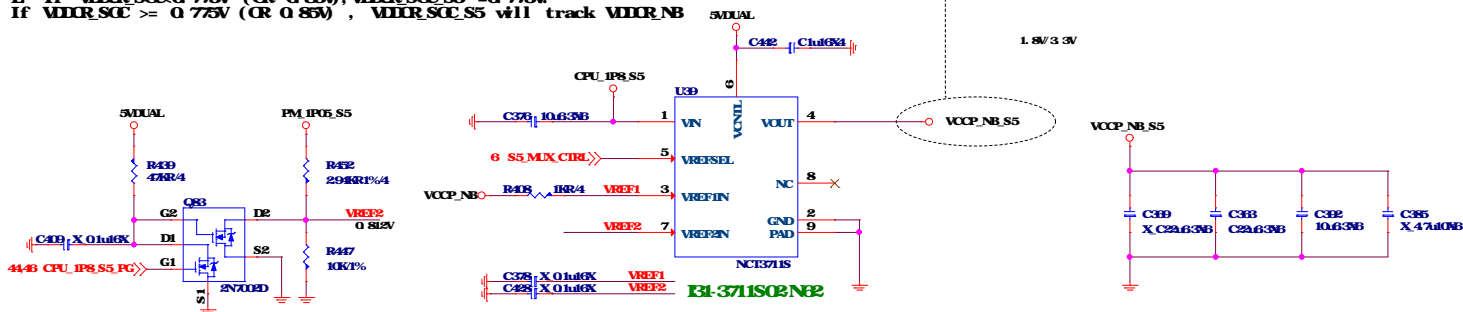
**FOR**  
**VCCP\_SOC\_s5**      **Q 9A**

**TYPEO Only**

**S5\_MX\_CTRL**  
**HGH S0**  
**LOW S3/S5**

**H +VDDR\_FCHALW will track VDNB**  
**L: If VDDR\_SCC<0 775V (OR 0 85V), VDDR\_SCC\_S5 =0 775V.**  
**If VDDR\_SCC >= 0 775V (OR 0 85V) , VDDR\_SCC\_S5 will track VDDR\_NB**

**(VIDCR\_SOC\_S5 is only used for AMD Family 15h Models 60h 6Fh processors) Bristol Ridge TYPE0**

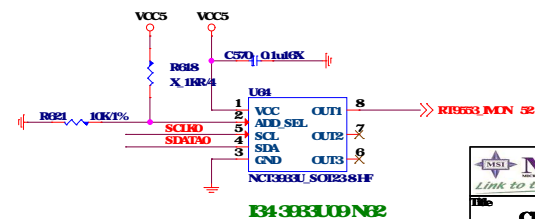
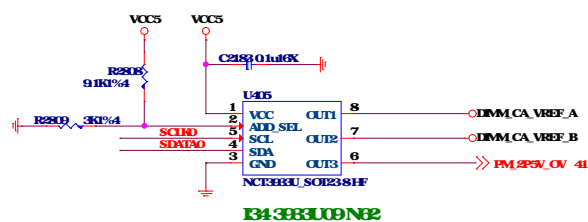
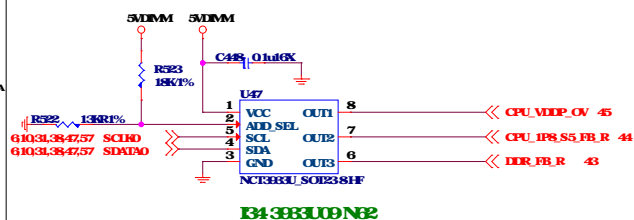


## Over Voltage Control IC

**0x26 RH=18K RL=13K**


**0x28 RH=9 1K RL=3K**

**0x2A: RH=OPEN RL=10K**

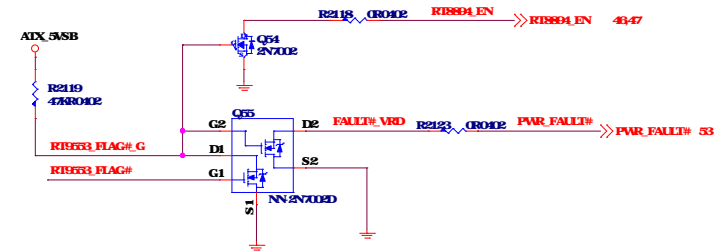
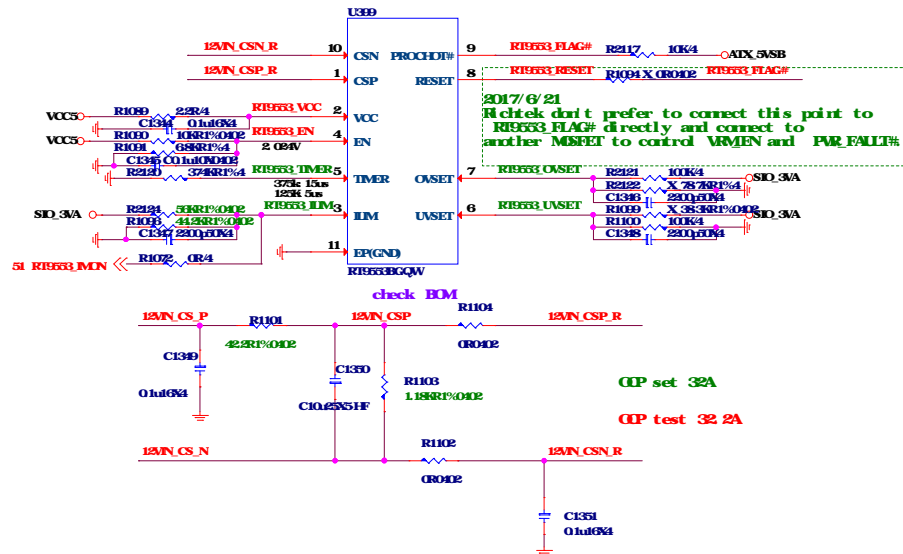


ADDRESS	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
RH(KOhm)	OPEN	39	3	22	13	10
RL(KOhm)	10	13	23	3	39	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

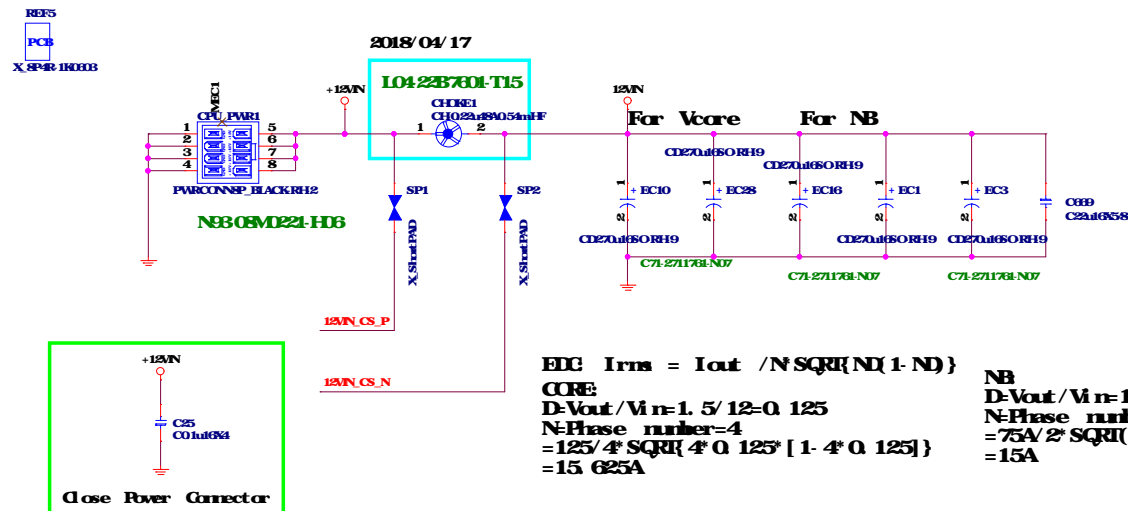
## UPI VOLTAGE CONSOLE

 <b>MSI</b> <small>THE MASTER OF QUALITY</small> <i>Link to the Future</i>				<b>MICROSTART INT'L CO., LTD.</b>			
<b>Title</b> <b>CPU Power/NB Switch/NCI3B33</b>							
<b>Size</b> Custom		<b>Drawnet Number</b> <b>MS-7869</b>				<b>Rev</b> <b>21</b>	
<b>Date</b> Wednesday, July 04, 2006		<b>Sheet</b> 51		<b>of</b> 68			

**VCORE EDC MAC 125A**  
**NB EDC MAX75A**



## CPU POWER CONNECTOR



$TDC_{Irms} = I_{out} / N \sqrt{ND(1-ND)}$   
**CORE:**  
 $D=V_{out}/V_{in}=1.5/12=0.125$   
 $N=$ Phase number=4  
 $=80/4 \sqrt{4 \times 0.125 \times [1 - 4 \times 0.125]}$   
 $=10A$

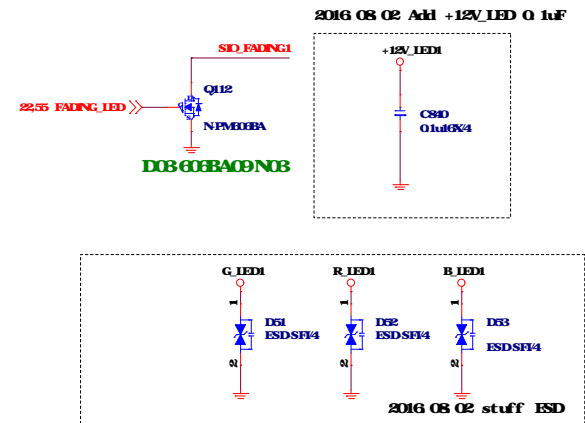
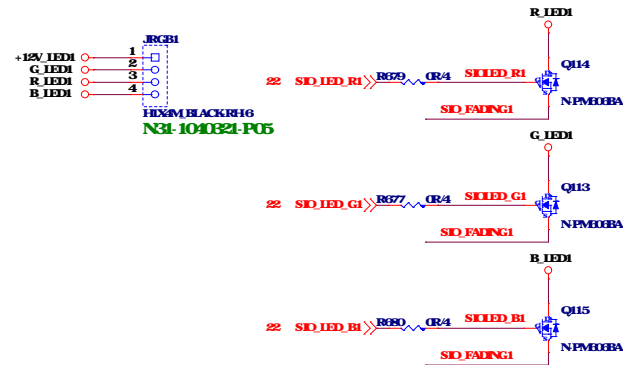
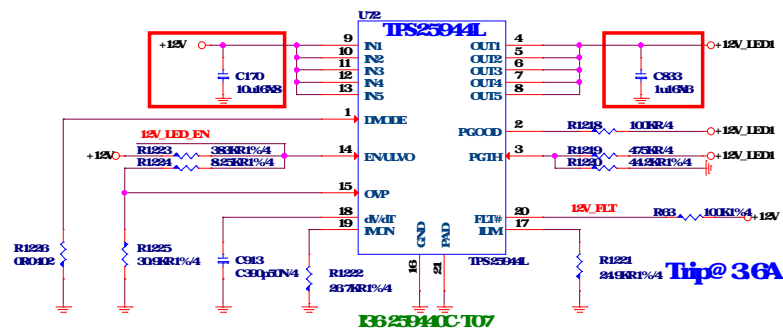
**NB**  
 $D = V_{out} / V_{in} = 1.2 / 12 = 0.1$   
**N-Phase number=2**  
 $= 654 \cdot 2^{\text{SQRT}(2^0 \cdot 1^* (1 - 2^* 0.1))}$   
**=13A**

EDC Irms = Iout / N\*SQR{ND\*(1-ND)}  
CORE:  
D-Vout/Vin=1.5/12=0.125  
N-Phase number=4  
=125/4\*SQR{4\*0.125\*[1-4\*0.125]}  
=15.625A

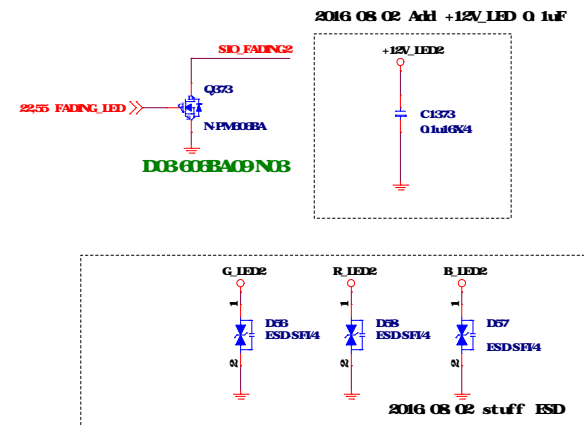
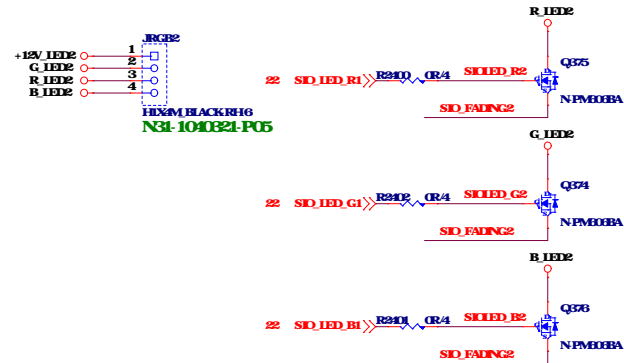
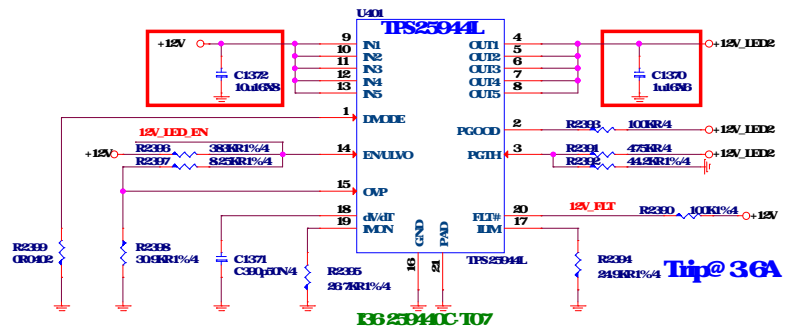
**NB**  
**D=Vout / Vi n=1. 2/ 12=0.1**  
**N=Phase number=2**  
**=75A/ 2\* SQRT(2\* 0.1\* (1- 2\* 0.1))**  
**=15A**



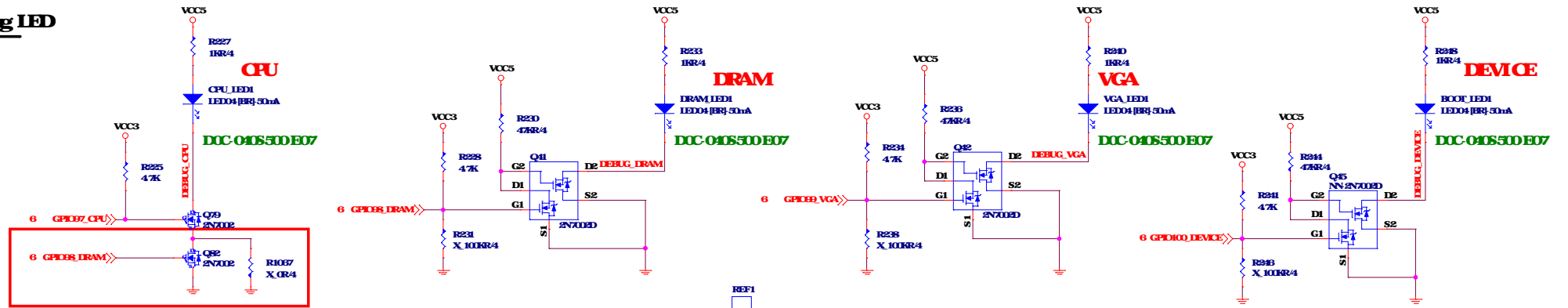
# LED Control by SIO



# LED Control by SIO

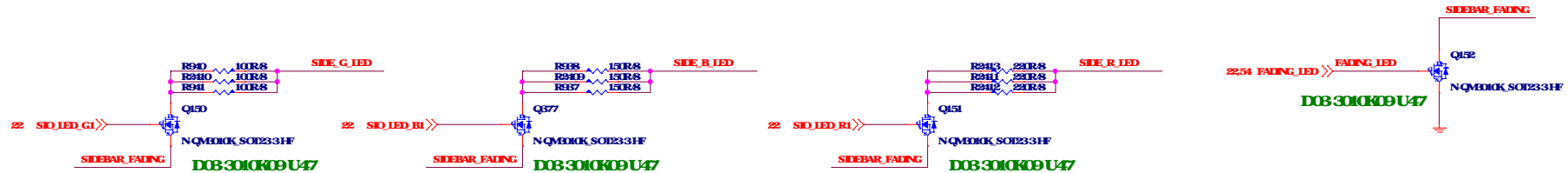
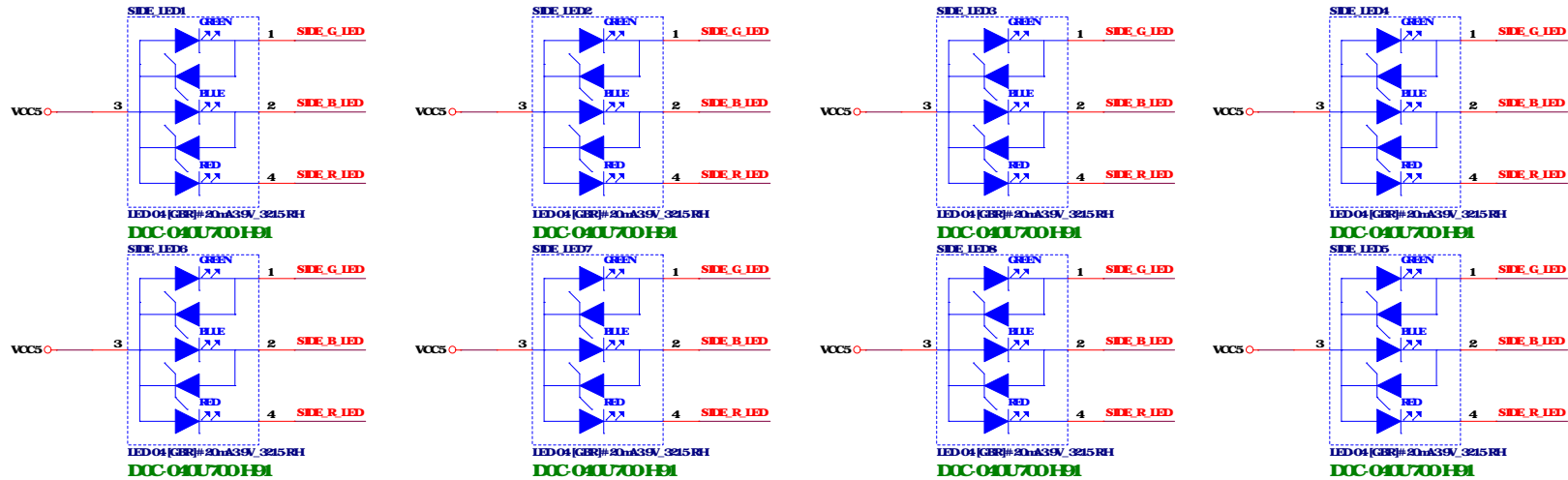


## EZ Debug LED

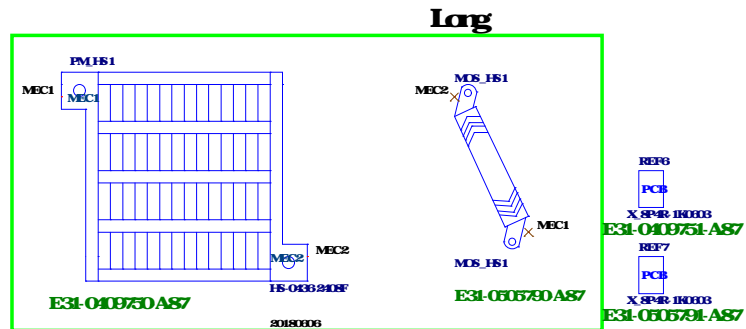


GPIO	GPIO7	GPIO8	GPIO9	GPIO10
LED	GPIO7	GPIO8	GPIO9	GPIO10
	GPIO7	GPIO8	GPIO9	GPIO10
	GPIO7	GPIO8	GPIO9	GPIO10
	GPIO7	GPIO8	GPIO9	GPIO10

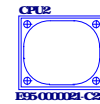
## BOARD SIDE LED



## HEAT SINK

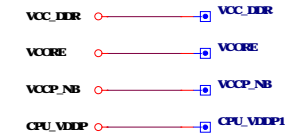
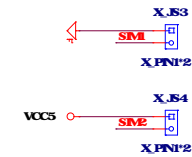


## CPU Socket

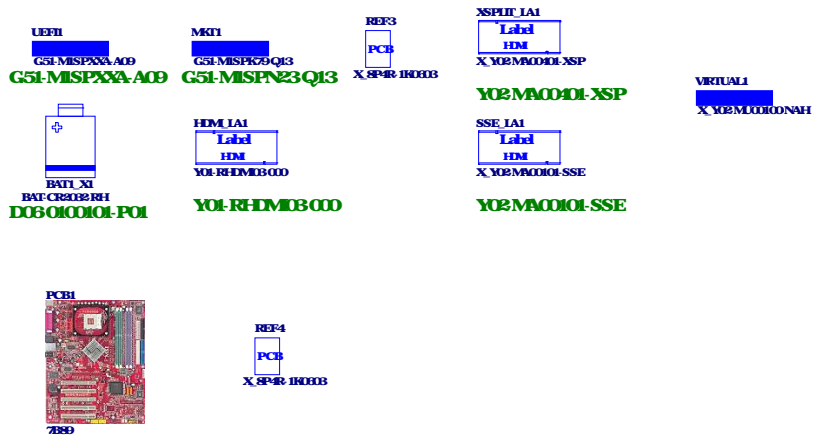


**RETENTION MODULE**  
**E95 000022 C22**

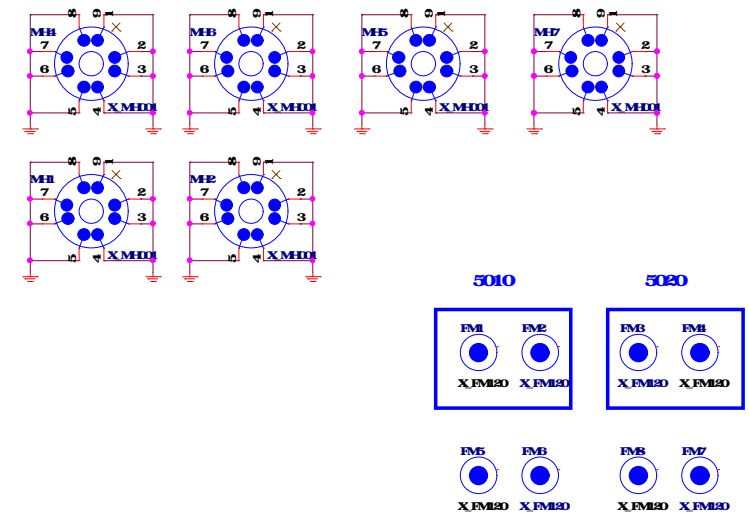
## Simulation



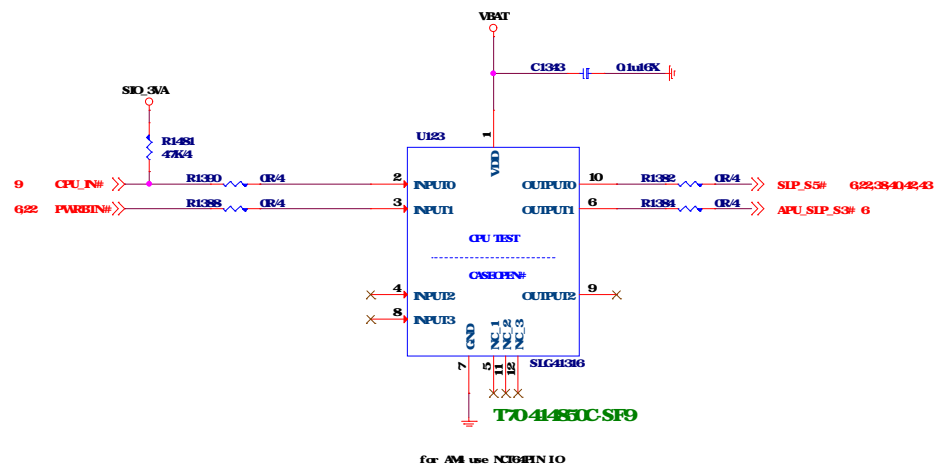
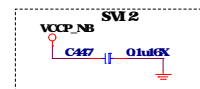
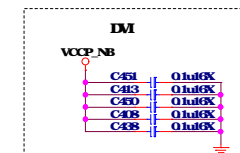
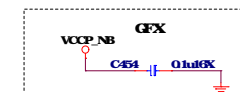
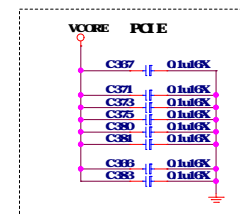
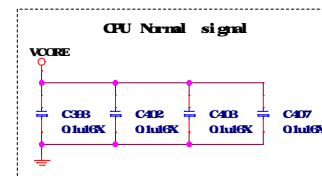
## MANUAL PART



## Optics Orientation Holes



OPT	Configure	BOM	Function
		601- 7A37- A01	XXXX

**Mat Cap**

### RTC & Clear CMOS Circuit

